


IEEE Build-Up Substrate Symposium (BUSS)




Substrate Materials for Advanced Packaging

Masato Fukui

Resonac Corporation

May 2nd, 2024

Today's Contents



1. Corporate Introduction
2. Introduction for Core & Prepreg for Advanced Package Substrate
 - Motivation and Challenges in Semiconductors
 - Resonac's Proposal for Market Requirement
 - Low CTE Materials
 - Super Flat Cores
3. Future Technology Roadmap

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January 2023: Resonac was Born RESONAC 4

The diagram illustrates the formation of Resonac. On the left, a blue rounded rectangle contains the text "Showa Denko". On the right, an orange rounded rectangle contains the text "Showa Denko Materials (Former Hitachi Chemical)". A blue arrow points from the "Showa Denko" box to the "Showa Denko Materials" box, and an orange arrow points from the "Showa Denko Materials" box to the "Showa Denko" box, with both arrows meeting at a central point. Below this, the Resonac logo is displayed in large blue letters, with the tagline "Chemistry for Change" underneath.

RESONAC
Chemistry for Change

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January 2023: Resonac was Born RESONAC 5

Resonate × **Chemistryの「C」**
共鳴する・響き渡る

RESONAC
 Chemistry for Change
 共創型化学会社
Co-Creative Chemical Company

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Strategy to Establish Competitive Advantage RESONAC 6

- Marketing, Research and Development -

Materials

Composite materials

Manufacturing

Evaluation and Simulation

Market

Access to downstream → **Clarifying customer needs**

Resin & Filler design Technology

Resin
Epoxy
Filler
Heat-dissipating filler

Formulation Technology
 Photosensitive insulation material
Copper clad laminate

Industrial Technology
 Solder resist
Molding compound

Film coating
Mixing
Filler dispersion

Evaluation Technology

Process solution
Simulation

2.x/3D packaging
Power device

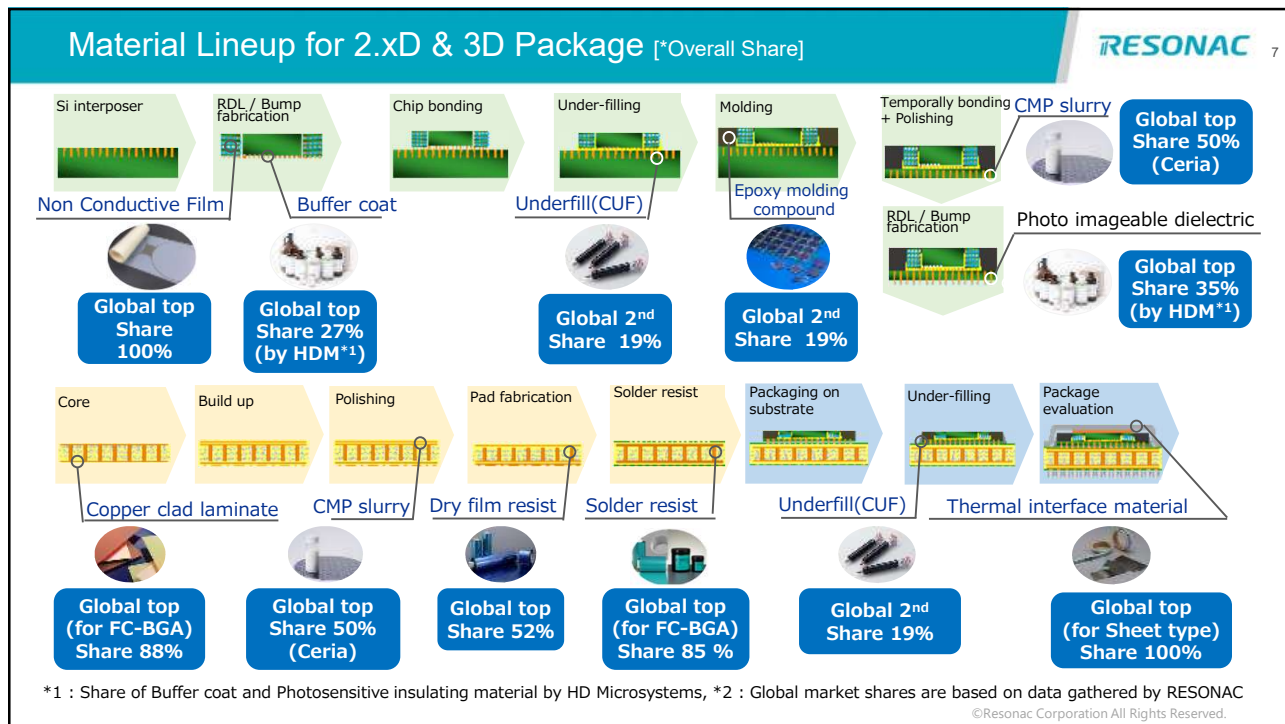
← **Innovation through reconciliation of wide-ranging technology** **Providing values** →

● Source of competitiveness

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www.ieee-buss.org

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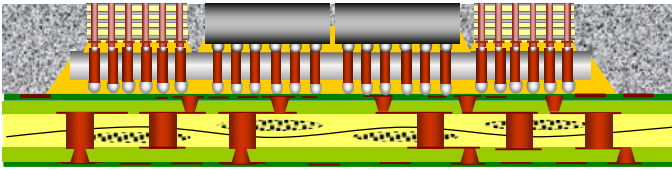
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Motivation and Challenges in Semiconductors



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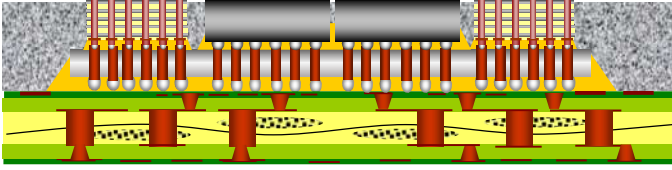


Motivation	Approach	Challenges
<i>High Speed</i>	<i>HSIO on Substrate</i>	<i>Signal Loss</i> → <i>Electrical Property, Body size</i>
<i>Large Capacity of Data Processing</i>	<i>Multi-Core on Die, Large Die</i> → <i>Yield, Manufacturing Cost</i>	<i>Complex Assembly</i> → <i>Chiplet</i> → <i>Power Delivery</i> → <i>Large Body Size</i>
<i>Low Power Consumption</i>	<i>Narrow Pitch</i> → <i>Bump Pitch Scaling</i>	<i>High Density Circuit</i>

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Resonac's proposal for Large Size Substrate



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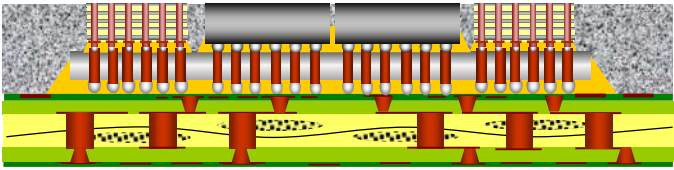


Challenge in Semiconductors	Requirement To Substrate	Breakthrough During Substrate Process	Proposal / Solution From Material Stand-point
<i>Large body size</i>	<i>Low Warpage</i> <i>High Yield</i>	<i>Warpage Control</i> <i>Shrinkage Control</i>	<i>Low CTE, High Modules</i> <i>Shrinkage Accuracy</i>
<i>High density circuit</i>	<i>Narrow pitch</i>	<i>Fine L/S Fabrication</i> <i>Narrow pitch TH</i>	<i>High Drill-processability</i>
<i>Electrical property</i>	<i>Signal Integration</i>	<i>Pattern, PKG Design</i>	<i>Low Dk/Df</i>
<i>Power delivery</i>	<i>More efficiency Power Delivery</i>	<i>Embedded Multi-layer core (MLC structure)</i>	<i>Super FLAT Core</i> <i>High Resin flow Prepreg</i>

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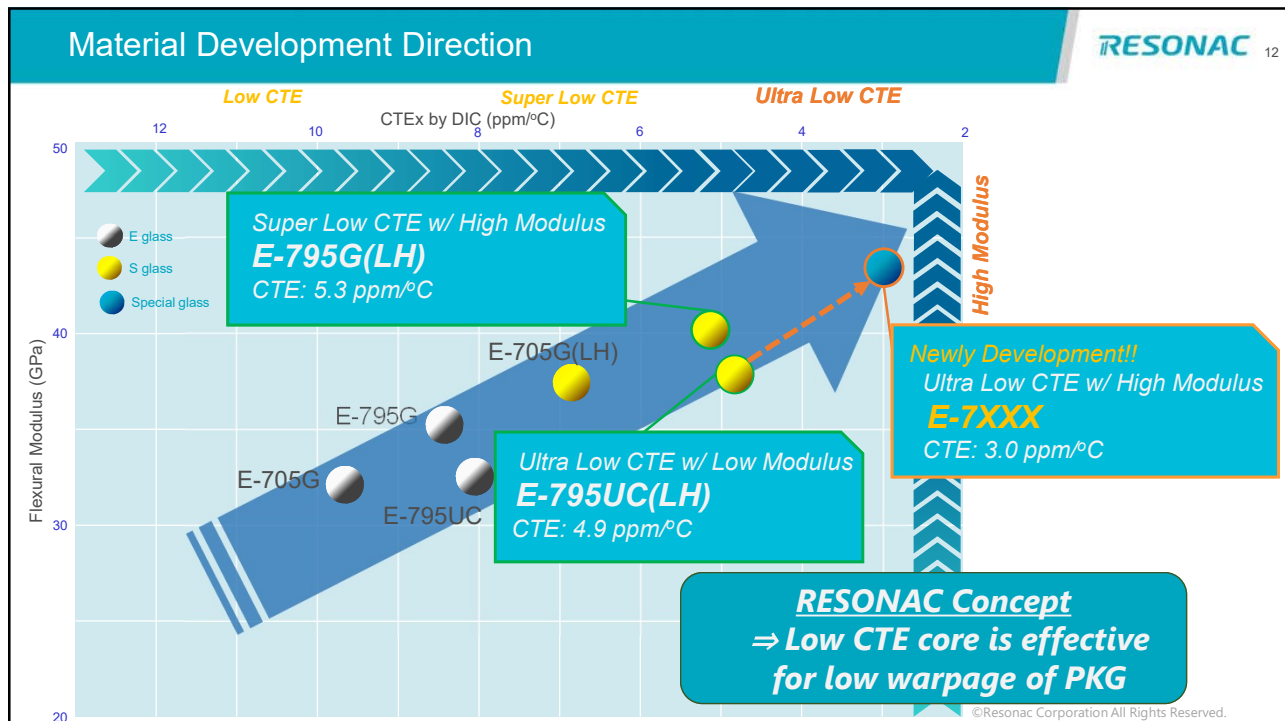
Resonac's proposal for Large Size Substrate

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Challenge in Semiconductors	Requirement To Substrate	Breakthrough During Substrate Process	Proposal / Solution From Material Stand-point
<i>Large body size</i>	<i>Low Warpage High Yield</i>	<i>Warpage Control Shrinkage Control</i>	<i>Low CTE, High Modulus Shrinkage Accuracy</i>
<i>High density circuit</i>	<i>Narrow pitch</i>	<i>Fine L/S Fabrication Narrow pitch TH</i>	<i>High Drill-processability</i>
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For Warpage Control [Material Properties, CTE]


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Item	Conditions		E705G		E795G		E795UC	
			E705G	E705G(LH)	E795G	E795G(LH)	E795UC	E795UC(LH)
Glass type	Glass type		E	S	E	S	E	S
	Weave density		Std	HD	Std	HD	Std	HD
Tg	TMA	°C	260	260	280	280	280	280
	DMA		300	300	330	330	330	330
CTE (Comp.)	$\alpha 1$ (X)	ppm/°C	9.5	7.2	8.0	5.6	7.5	4.9
	$\alpha 2$ (X)		1.1	1.0	1.0	1.0	1.0	1.0
CTE (DIC)	140-180°C	ppm/°C	9.6	6.9	8.5	5.5	8.1	4.9
	180-220°C		10.3	7.2	8.9	6.0	8.0	4.9
Peel Strength	12 μ m	kN/m	0.9	0.9	0.7	0.7	0.7	0.7
Flexural Modulus	A	GPa	33	38	36	41	33	38
Dk	1 GHz	-	4.5	4.2	4.4	4.2	4.2	4.0
Df	1 GHz	-	0.008	0.008	0.006	0.006	0.009	0.009

*1; For 800 μ m thickness
*2; Dk/Df measured by SPDR method.

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For Warpage Control [Warpage Simulation]

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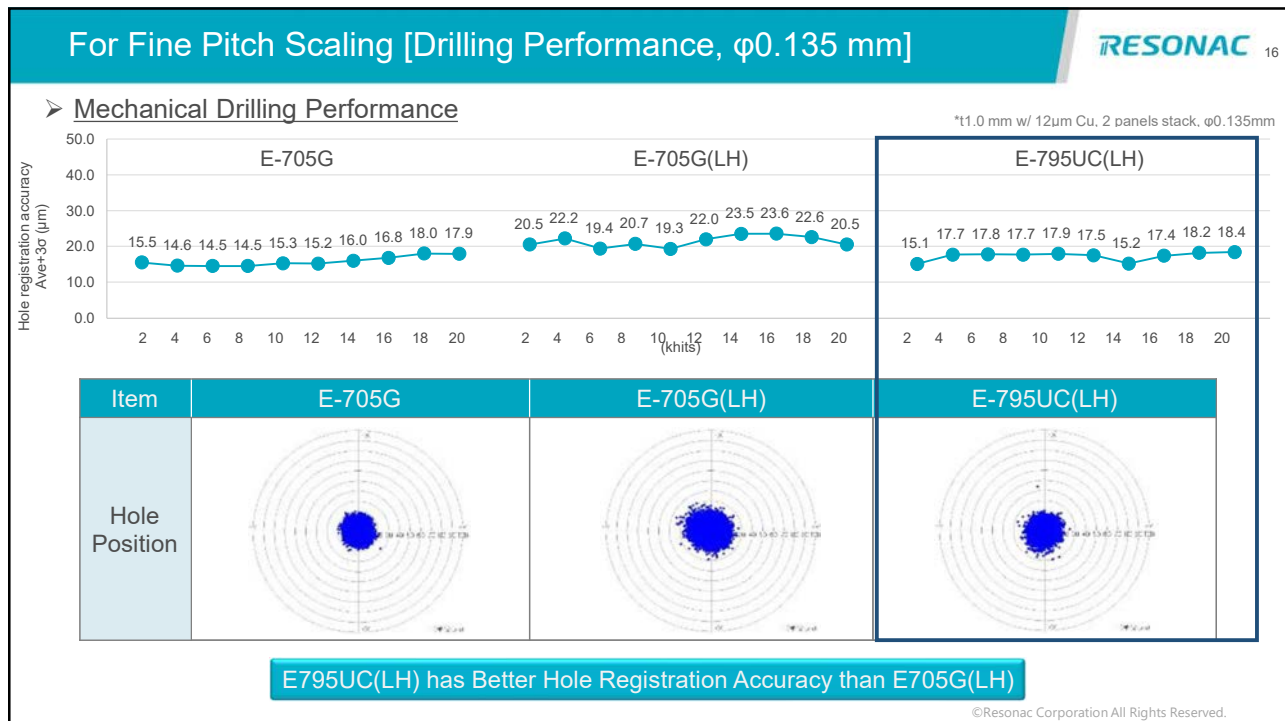
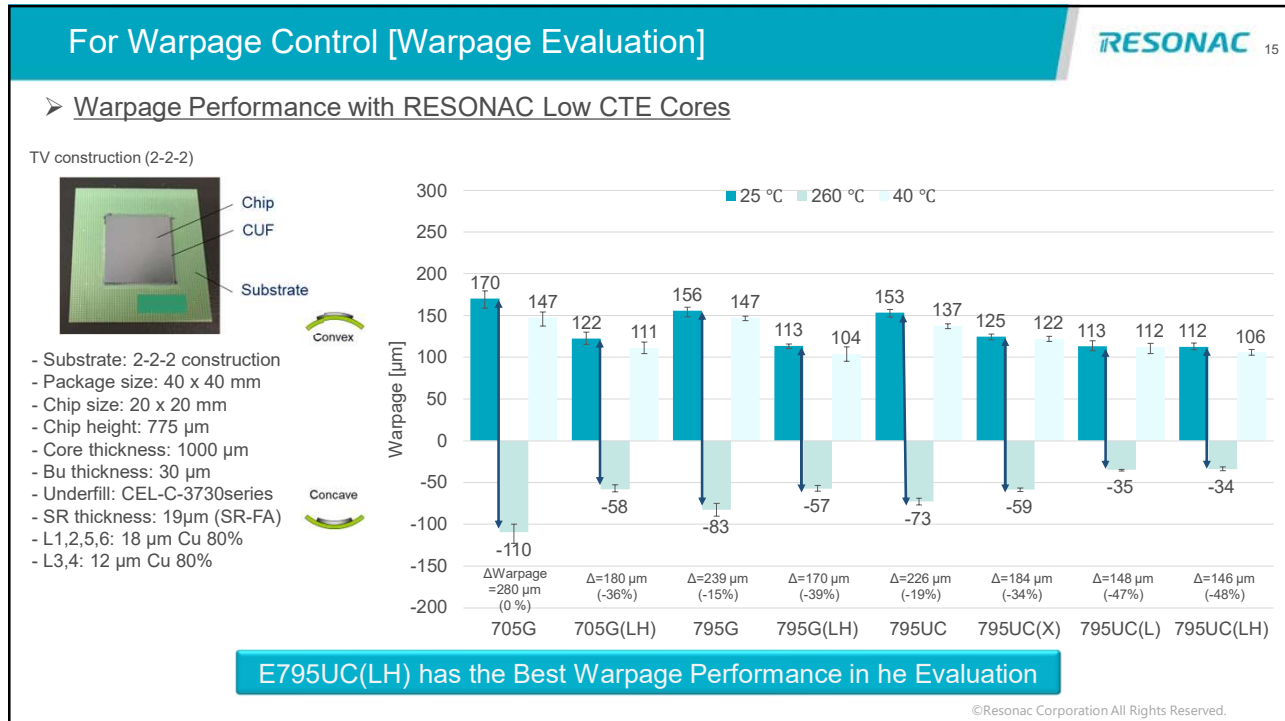
➤ Warpage Simulation Results with Each Material Set and Thickness Variation

- Simulation method: 3D elastic analysis
 Δ Warpage: Difference between 25 °C and 260 °C
 Benchmark: 705G(LH) 800 μ m
- Simulation model
 - Substrate: 5-2-5 construction
 - Package size: 60 x 60 mm
 - Die size: 25 x 25 mm
 - Die height: 725 μ m
 - Bu thickness: 30 μ m
 - Underfill thickness: 80 μ m (CEL-C-3730S-012L3-20)
 - SR thickness: 20 μ m (SR7300)
 - Cu thickness: 18 μ m
 - Cu coverage: 80%


Core thickness (μ m)	Δ Warpage index				
	705G(LH)	795G(LH)	795UC	795UC(X)	795UC(LH)
200	2.04	1.88	2.17	2.05	1.87
400	1.55	1.36	1.70	1.56	1.33
600	1.23	1.04	1.38	1.24	1.00
800	1.00	0.82	1.15	1.01	0.78
1000	0.83	0.67	0.97	0.84	0.63
1200	0.71	0.56	0.83	0.71	0.51
1400	0.61	0.47	0.72	0.62	0.43
1600	0.53	0.41	0.64	0.54	0.36

Warpage Performance in Thickness Variation can be simulated by RESONAC Technology.

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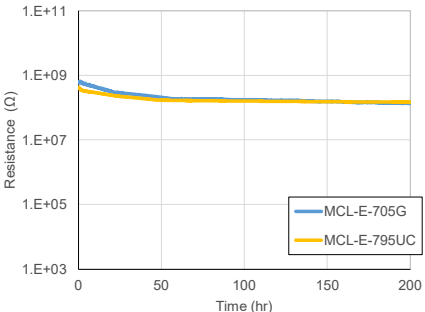
For Fine Pitch Scaling [Reliability of Through Hole]

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➤ Reliability Testing Results for Narrow Pitch Through Hole

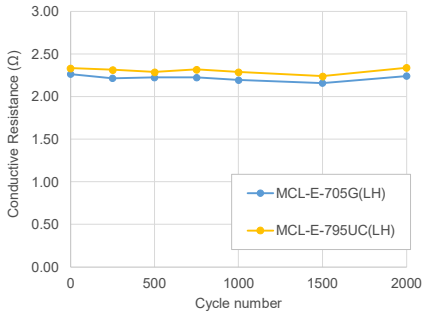
[B-HAST]

- Thickness: 1.01 mm
- TH diameter: 150 μm
- Wall to Wall: 100 μm
- Condition: 130 °C/85 %RH/3.5 V



[Thermal Cycle Test]


- Thickness: 1.01 mm
- TH diameter: 150 μm
- Wall to Wall: 150 μm
- Condition: -55 °C/30 min \leftrightarrow 125 °C/30 min

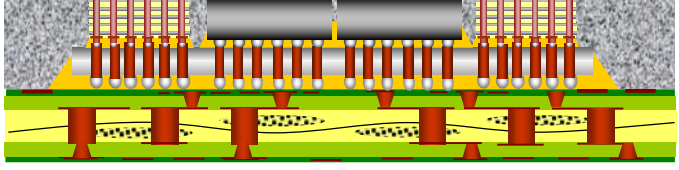


RESONAC Materials show the excellent reliability with Narrow Pitch Through Hole.

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Resonac's proposal for Large Size Substrate


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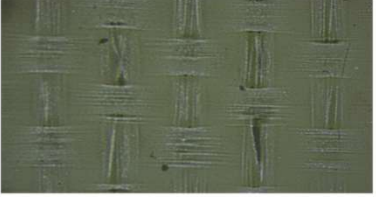
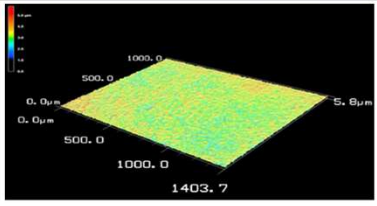
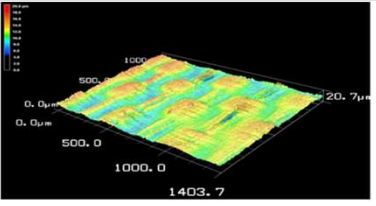
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Technology of Super Flat Core & Prepreg

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■ **Feature**
 - Smooth surface - Small thickness variation
 - Good filling capability - Stable dimension change

Item	TYPE F	Current-type
Prepreg surface		
Laser micro scope (KEYENCE, VK-X100)		

TYPE-F Technology can Uniformly Coat the Resin on the Glass Cloth

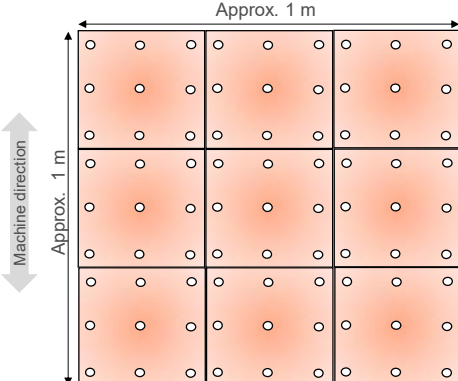
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For Fine Pitch Scaling

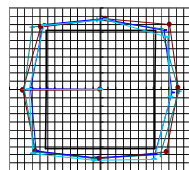
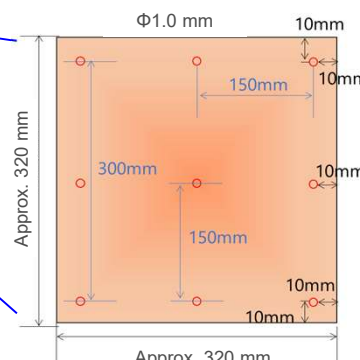
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➤ Thermal Strain Measurement Method
■ **Measurement method : MCL-E-795G(LH) 1.0 mm Core**

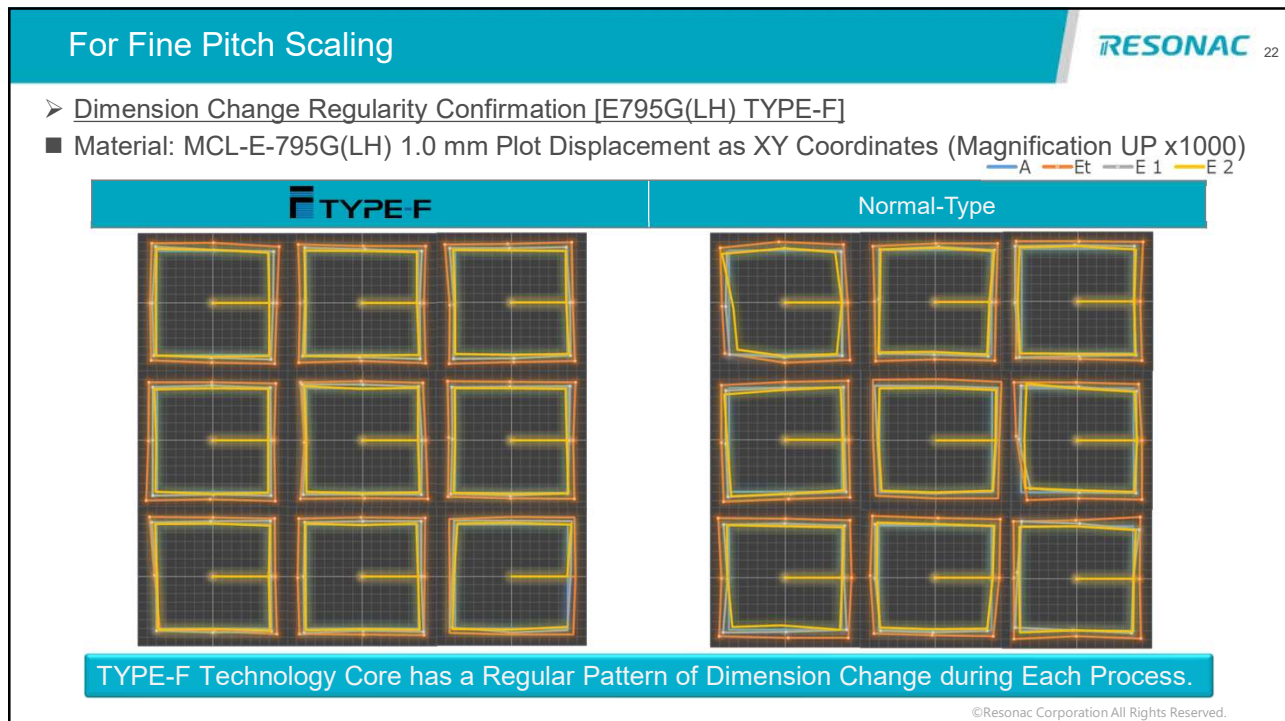
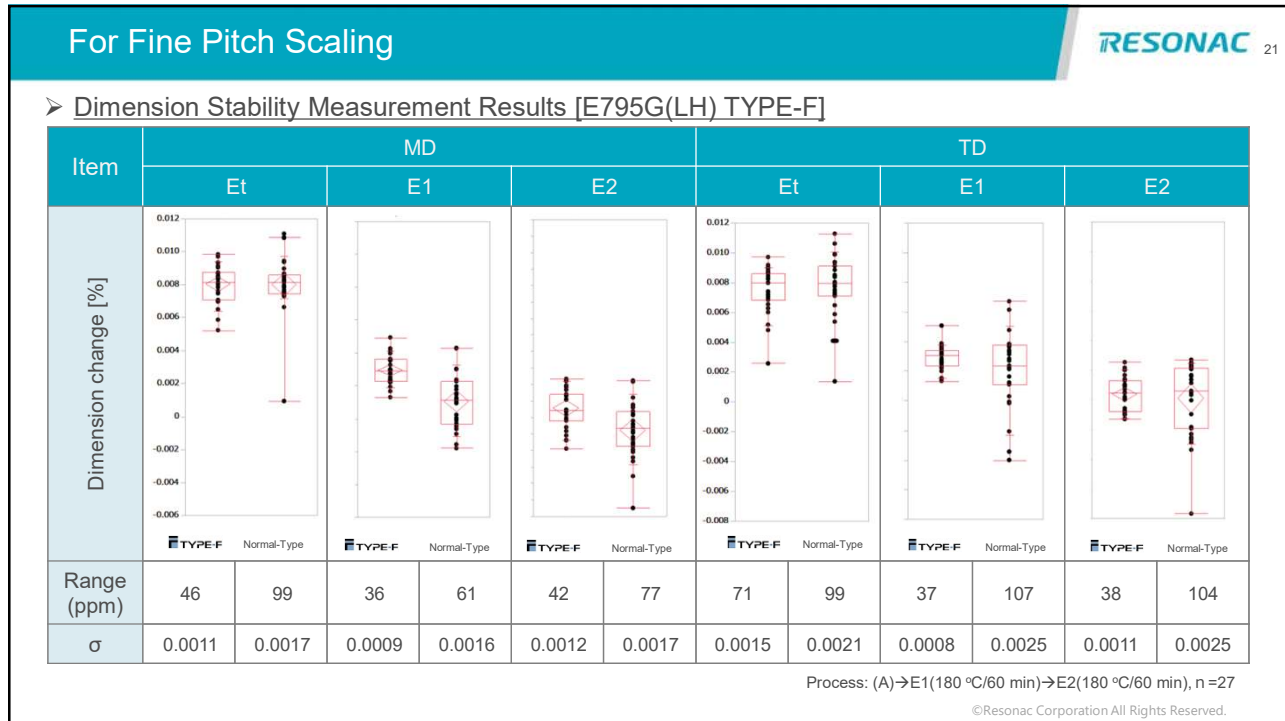
- 1) Divided into 9 pcs from master size
- 2) $\phi 1\text{mm}$ TH at even positions
- 3) Measure the distance between TH / TH
- 4) Perform heat treatment and measure the distance between TH and TH

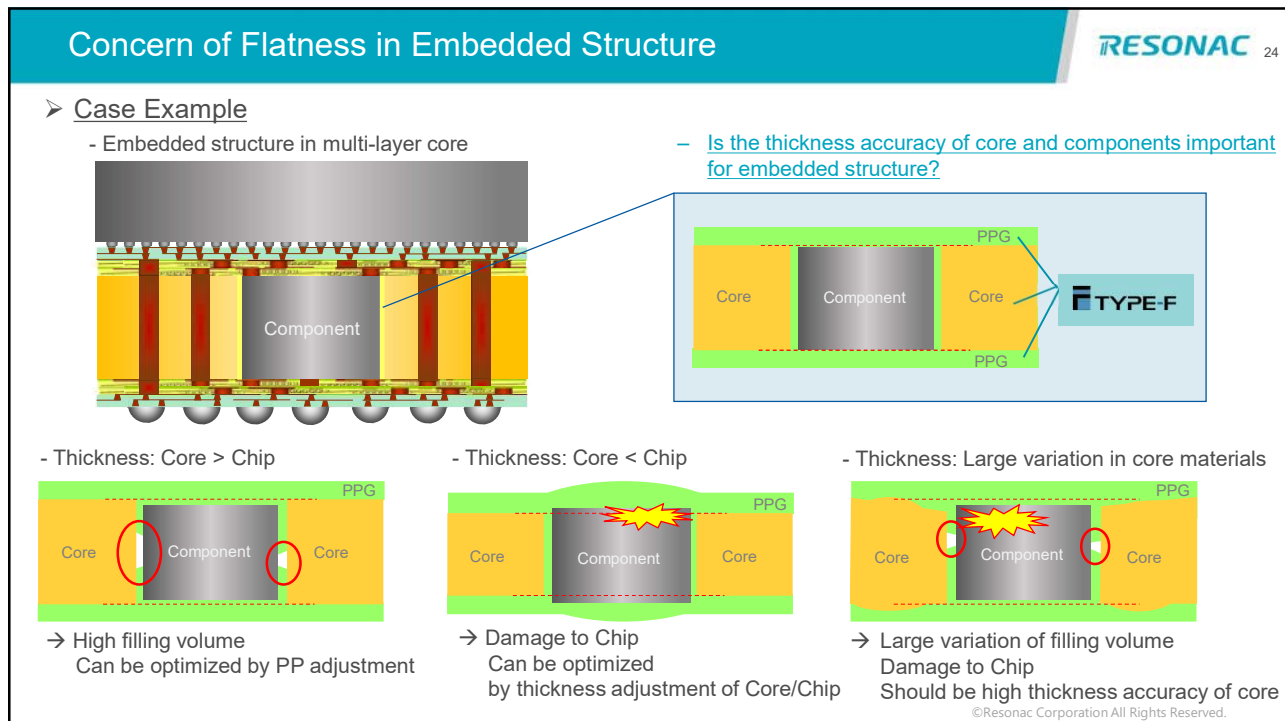
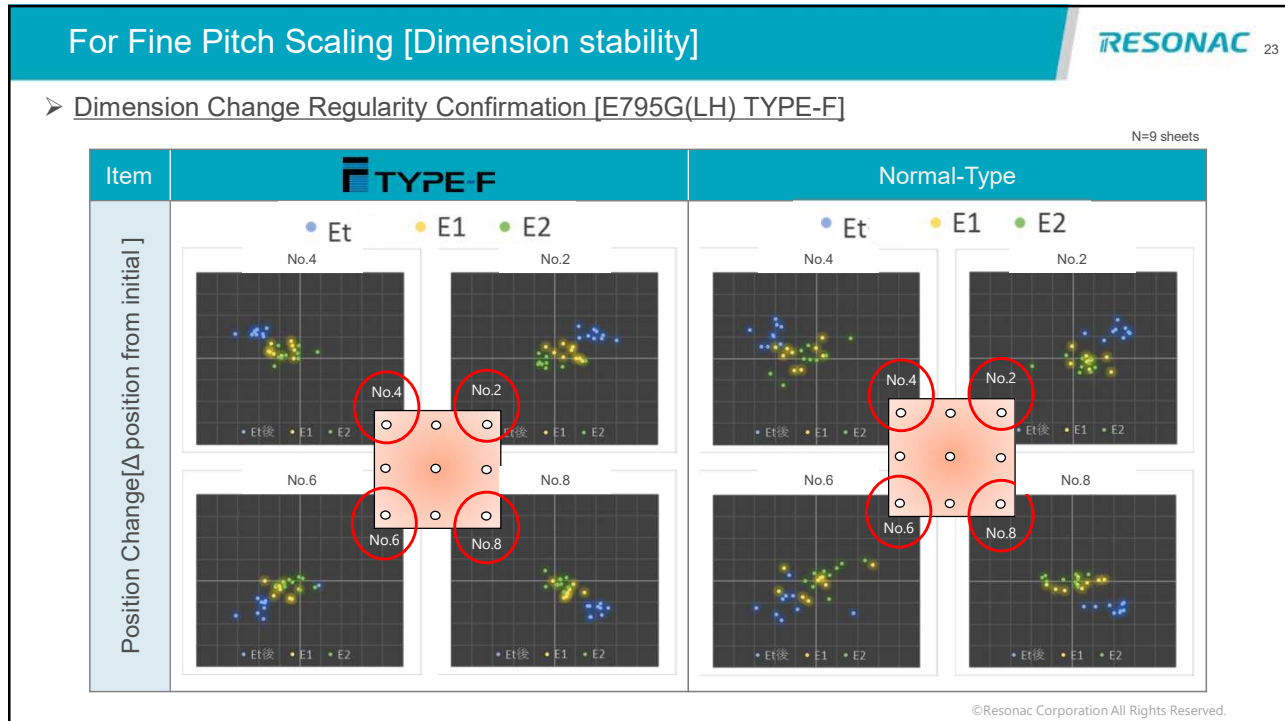


◆ Thermal strain data image
 -Plot displacement as XY coordinates (Magnification UP)

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For Embedded Structure

➤ LTV Thickness Distribution Measurement Method

- Material: E705G t1.0 mm
- Measurement method

- 1) Panel size: 500x500mm
[Divided into 4 pcs from master sheet size Approx. 1 m²]
- 2) Measured the thickness every 40 mm distances both vertical and horizontal direction by a micrometer

- ◆ Thickness distribution
All area : 144 point
Center area : 100 point
Edge area : 44 point
- ◆CTV (Chip area thickness variation)
Calculated the thickness difference between adjacent 4 points (Max – Min)
All area : 121 point
Center area : 81 point
Edge area : 40 point

□ □ □ * Calculated the thickness difference between 4 points

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For Embedded Structure

➤ LTV Thickness Distribution Measurement Method

- Material: E705G t1.0 mm

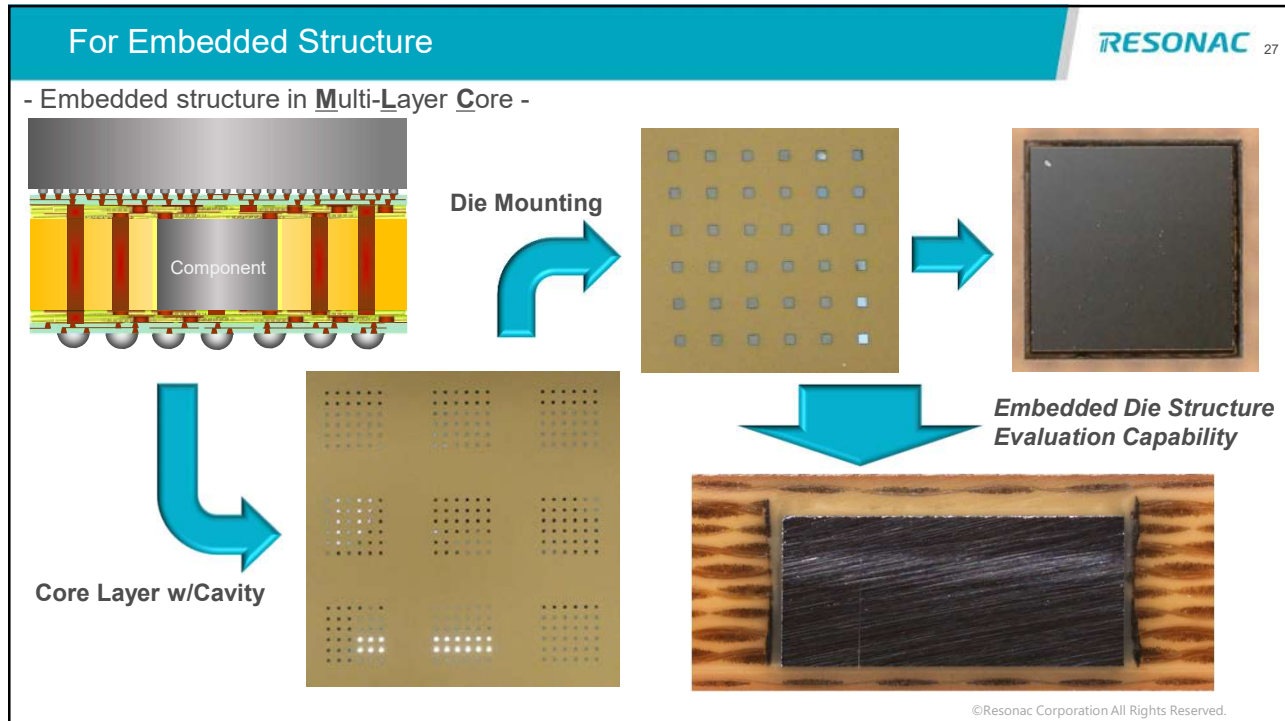
All area

Center area

Edge area

		TYPE F	Normal-Type	TYPE F	Normal-Type	TYPE F	Normal-Type
LTV Ave	[μm]	2.17	3.04	2.39	2.53	1.73	4.10
LTV Std.	[μm]	1.07	2.31	1.09	1.64	0.88	3.04
LTV Max	[μm]	5	14	5	10	4	14

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The data shown here are based on technical information and data available as of Jan. / 2023 and not intended to guarantee the quality.