Advanced Electroplating Process for IC Substrates
Sam Dharmarathna
Line of Business R&D – IC Substrates

MacDermid Alpha Electronics Solutions

$1.4 B
2023 NET SALES

>30 COUNTRIES
WITH FACILITY OPERATIONS

>6,800
CUSTOMERS WORLDWIDE

>2,200
EMPLOYEES
We are INTEGRAL to Electronics Manufacturing

Our Product Offerings
A Full Portfolio to Support the Electronics Manufacturing Industry
Additives Tailored to Customer Needs

- In-House synthesis - Libraries of Additive Molecules
  - Develop and maintain comprehensive collections of additive molecules to reduce the time from conception to market.

- Novel Molecules – IP Protection
  - Create innovative molecules with the potential for intellectual property protection.

- Fine Tune Performance – Fine L/S
  - Ability to modify the electro-chemical properties of additives and physical/mechanical properties of deposit leading to robust plating formulations.

Tailored Formulations To Enable Specific Technologies

- Ability to Modulate – Flat vs. Domed
  - Develop molecules that enable the modulation of surface profiles.

- Mitigate Defects - Reliability
  - Proprietary blend of functional groups in the molecules to control grain refinement and final grain structure.

- Deposit Properties - Mechanical, Physical & Purity
Plating Tools for Advanced Packaging

- Electrodeposition for advanced L/S requires precise coordination and cadence between equipment and additives to achieve optimal performance.
- Modern tools utilize unique mass transfer methods as opposed to conventional VCP systems.

- Better understanding of tools and additives leads to more robust formulations.

IC Substrate Technology

- Higher functionality with more components in a “package”
  - Sensors, memory, logic, CPU
  - PoP, SiP, etc.
- Transition from wire bonding to flip chip designs
  - Reduced chip area
  - Increased I/O count
  - Reduced inductance
  - Higher signal speeds
  - Improved heat management
- Still need to route signals out of the die to the component substrate for connection to the PCB.
Deposition Mechanism

- Bath composition
  - Lower $\text{H}_2\text{SO}_4$ to reduce solution conductivity and promote larger difference in potentials
  - Higher $\text{CuSO}_4$ to increase filling speed
  - Chloride ions provide adsorption sites

- Additives
  - Suppressor preferentially adsorbed on the surface
  - Brightener diffuses to the bottom of the microvia
  - Leveler selectively adsorbs on the high current areas

- Fill progression
  - Plating at via bottom is fastest at the beginning
  - As plating proceeds, the potential differences and plating rate difference of surface and microvia lessen
  - Once filled, all plating rates are similar

Systek UVF 200 Process Overview

- DC Acid Copper plating process specifically designed for 2-in-1 RDL applications for FCBGA

  - Pattern plate process
  - High coplanarity of traces and pads
    - Typically, <2 μm R-Value
  - Highly controlled trace profile
    - Typically, <15%
  - Via Fill
    - Up to 60 μmØ x 30-35 μm deep
    - Dimple: <5 μm, Overfill <3 μm
    - Surface Copper: 10-15 μm

- Compatible with High-Speed Plating Tools
  - ASM-NEXX Stratus P500
  - Semsysco
Capabilities

- Panels with different designs, feature sizes, and copper thickness specifications were plated during the evaluation

<table>
<thead>
<tr>
<th>Features/Spec</th>
<th>Design 1</th>
<th>Design 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line/Space</td>
<td>9/12 μm</td>
<td>15/20 μm</td>
</tr>
<tr>
<td>BMV Diameter</td>
<td>40 μm</td>
<td>49 μm</td>
</tr>
<tr>
<td>BMV Depth</td>
<td>15 μm</td>
<td>20 μm</td>
</tr>
<tr>
<td>Plating Thickness</td>
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<td>17 μm</td>
</tr>
<tr>
<td>Plating Time</td>
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<td>15 minutes</td>
</tr>
<tr>
<td>Current Density</td>
<td>4-5 ASD</td>
<td>5-6 ASD</td>
</tr>
<tr>
<td>Dimple</td>
<td>± 2 μm (POR)</td>
<td>± 2 μm (POR)</td>
</tr>
<tr>
<td>Uniformity (W/L)</td>
<td>2 μm (POR)</td>
<td>&lt;5 μm (POR)</td>
</tr>
<tr>
<td>Uniformity (W/P)</td>
<td>&lt;15% (POR)</td>
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</tr>
<tr>
<td>Anode</td>
<td>Insoluble</td>
<td>Insoluble</td>
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- 9 areas were measured on each side of the panel
- The best result was with 200/120/50 VMS
Substrate Design 1 Results
Copper Thickness vs Feature, VMS

- The average $R_{WID}$ was calculated via the difference on the plated height between fine line and pad/filled via.
- R-value improved with lower copper sulfate and higher sulfuric acid.
- WID uniformity was < 2 um with copper sulfate concentration < 200 g/L.
- WID uniformity was further improved with additional sulfuric acid.
Capabilities

• Panels with different designs, feature sizes, and copper thickness specifications were plated during the evaluation.

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</tr>
<tr>
<td>Uniformity (WIU)</td>
<td>2 μm ± 4 μm (POR)</td>
<td>&lt;5 μm ± 8 μm (POR)</td>
</tr>
<tr>
<td>Uniformity (WIP)</td>
<td>&lt;15% ± 20% (POR)</td>
<td>&lt;15% ± 20% (POR)</td>
</tr>
<tr>
<td>Anode</td>
<td>Insoluble</td>
<td>Insoluble</td>
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• 9 areas were measured on each side of the panel by ZYGO profiler
• The best result was with 200/120/50 VMS.

Substrate Design 2 Results
Copper Thickness vs Feature, VMS
Substrate Design 2 Results

Uniformity

- The average $R_{WID}$ was calculated via the difference on the plated height between fine line and pad/filled via
- $R$-value improved with lower copper sulfate and higher sulfuric acid
- WID uniformity was $< 5$ µm with copper sulfate concentration $< 240$ g/L

Via Fill Results

- Via size: 40x15 µm
- Plated thickness: 12 µm
- All conditions resulted in a bump on the filled vias
- As Cu was reduced and acid was increased, the domes on the filled vias decreased and the uniformity improved (reduced R values)

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<th>VMS</th>
<th>Bump (µm)</th>
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<td>240/40/50</td>
<td>3.8</td>
</tr>
<tr>
<td>200/120/50</td>
<td>0.9</td>
</tr>
</tbody>
</table>
SIMS Analysis

- Low impurities co-deposit with Cu
  - Electrical conductivity, grain structure, Cu reduction during SAP / mSAP, physical properties

Properties of Deposit

- Physical properties exceeded IPC class III specifications
- Deposit had equiaxial grain structure

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<tr>
<th>Plating Condition</th>
<th>2.0 ASD, 25°C</th>
<th>4.5 ASD, 35°C</th>
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<tbody>
<tr>
<td>Elongation (%)</td>
<td>22.0</td>
<td>20.1</td>
</tr>
<tr>
<td>Tensile Strength (kPSI)</td>
<td>40.4</td>
<td>40.4</td>
</tr>
<tr>
<td>Internal Tensile Stress (kg/mm²)</td>
<td>0.87</td>
<td>0.85</td>
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UVF 200 Summary

- Systek UVF 200 is a versatile plating process for the 2-in-1 RDL plating of fine lines and filling of microvias in build up layer applications
  - Filling of microvias up to 60 μmØ x 30 μmD
  - Plating thickness of 15-18 μm within 15–20 min plating time
  - Low R-values between various features
  - Good within device (WID) and within panel (WIP) uniformity
- Process is very stable and tunable
  - Wide VMS operating range
  - Wide operating current density range
  - Compatible with Nafion membranes
  - All additives are CVS analyzable and controllable

Next Gen RDL Plating
Systek UVF 300

- Reduced variation in copper thickness
- High coplanarity across a wide range of current density
- Consistent via fill
Contact Us

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