






Advanced Electroplating Process for IC Substrates



Sam Dharmarathna
Line of Business R&D – IC Substrates



CONFIDENTIAL

MacDermid Alpha Electronics Solutions

-  **\$1.4 B**
2023 NET SALES
-  **>30** COUNTRIES
WITH FACILITY OPERATIONS
-  **>6,800**
CUSTOMERS WORLDWIDE
-  **>2,200**
EMPLOYEES



CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions 2

We are INTEGRAL to Electronics Manufacturing

ASSEMBLY SOLUTIONS

- Solder Pastes
- Wave Solder & Fluxes
- Solder Preforms
- Specialty Alloys
- Underfill / Encapsulant

SEMICONDUCTOR SOLUTIONS

- Photomask Imaging
- Chip Attach / Reform Fluxes, Solder Ball / Attach Flux
- Die Attach Paste / Film
- Fine Pitch and Particle SiP Solder Paste
- Die and Cu Clip Attach Paste / Film / Preforms
- Damascene Copper
- RDL, Pillar, and Bump Metallization
- Thermal Interface Materials / Fluxes / Preforms
- Wafer Level Backside Metallization
- Stiffener and Lid Seal Adhesives

CIRCUITRY SOLUTIONS

- IC Substrate Metallization
- QFN Adhesion
- QFN Tin Plating
- Through Hole Metallization
- Innerlayer Processing
- Copper Via Plating
- Full Build Copper Plating
- Solderable Finishes

CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

3

Our Product Offerings

A Full Portfolio to Support the Electronics Manufacturing Industry

Primary Metallization

- Direct Metallization
 - Wet Etch Graphite DM
 - Dry Etch Carbon and Graphite DM
- Electroless Copper
 - Stress-free Electroless Copper and SAP Copper

Electrolytic Metallization

- Electrolytic Coppers
- High Throw DC
- Periodic Pulse Reverse
- Via Fill / Through Hole Fill
- RDL 2-in-1

Circuit Formation

- Copper Adhesion Promotion
- High Throw DC
- Periodic Pulse Reverse
- Via Fill / Through Hole Fill
- RDL 2-in-1
- Component Termination Solderability
- Molded Interconnect Devices
- Light Emitting Diodes
- Solar Cell Metallization

Final Finishes

- Organic Solderability Preservative
- Immersion Tin
- Immersion Silver
- Electroless Nickel
- Immersion Gold (ENIG)
- Electroless Nickel
- Electroless Palladium
- Immersion Gold (ENEPIG)

Connector Finishes

- Electroplate
 - NiAu, NiPd
 - Ag/SnAg
 - Rd, Ru
 - NiW
 - Cu
 - Indium
 - NiP

Memory Disk

- Pre-clean and Zincate Solutions for Al substrate
- High Quality EN
- High Corrosion Resistance
- Low Particle Inclusion (PDI)
- Low Pit Count

Inks & Pastes

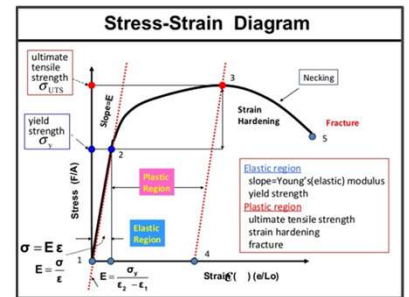
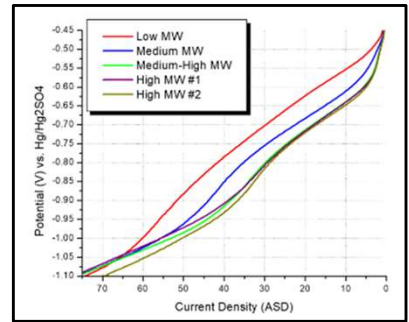
- MicroCat Conductive Ink
- ActiveCopper Paste
 - Copper Coin
 - Through Hole Fill for Power

CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

Additives Tailored to Customer Needs

- **In-House synthesis - Libraries of Additive Molecules**
 - Develop and maintain comprehensive collections of additive
Reduce the time from conception to market.
- **Novel Molecules – IP Protection**
 - Create **innovative molecules** with the potential for intellectual property protection.
- **Fine Tune Performance – Fine L/S**
 - Ability to modify the **electro-chemical** properties of **additives** and **physical/mechanical properties** of **deposit** leading to robust plating formulations.



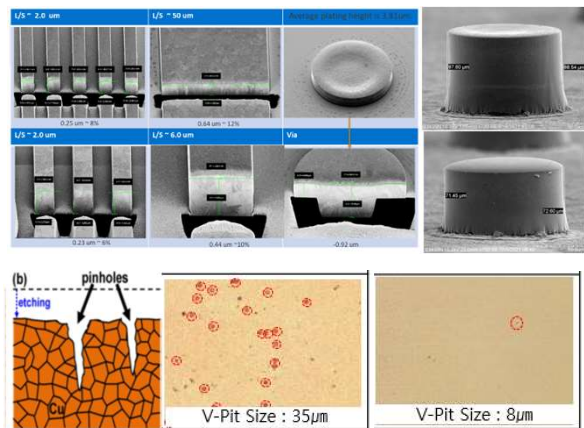
CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

5

Tailored Formulations To Enable Specific Technologies

- **Ability to Modulate – Flat vs. Domed**
 - Develop molecules that **enable the modulation** of **surface profiles.**
- **Mitigate Defects - Reliability**
 - **Proprietary blend of functional groups** in the molecules to control grain refinement and final grain structure
- **Deposit Properties - Mechanical, Physical & Purity**



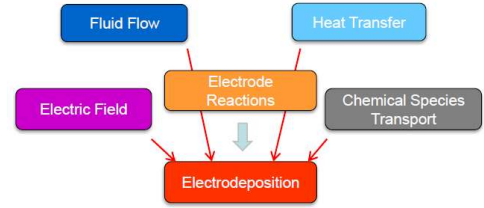
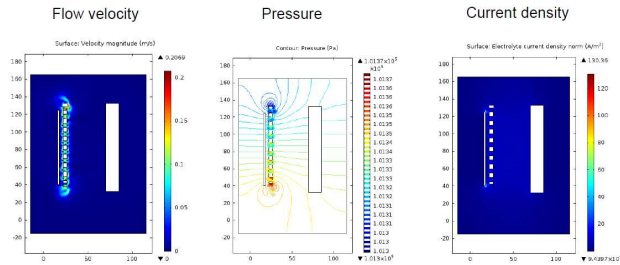
CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

6

Plating Tools for Advanced Packaging

- **Electrodeposition** for advanced L/S requires precise **coordination and cadence** between **equipment and additives** to achieve optimal performance.
- Modern tools **utilize unique mass transfer** methods as opposed to conventional VCP systems



- **Better understanding of tools and additives** leads to more **robust formulations**



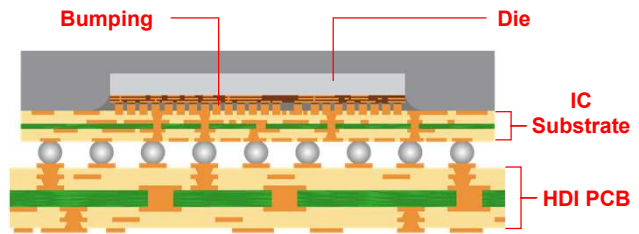
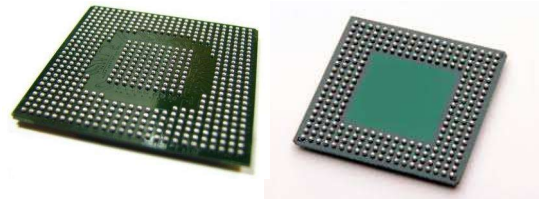
CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

7

IC Substrate Technology

- Higher functionality with more components in a “package”
 - Sensors, memory, logic, CPU
 - PoP, SiP, etc.
- Transition from **wire bonding to flip chip** designs
 - Reduced chip area
 - Increased I/O count
 - Reduced inductance
 - Higher signal speeds
 - Improved heat management
- Still need to route signals out of the die to the component substrate for connection to the PCB



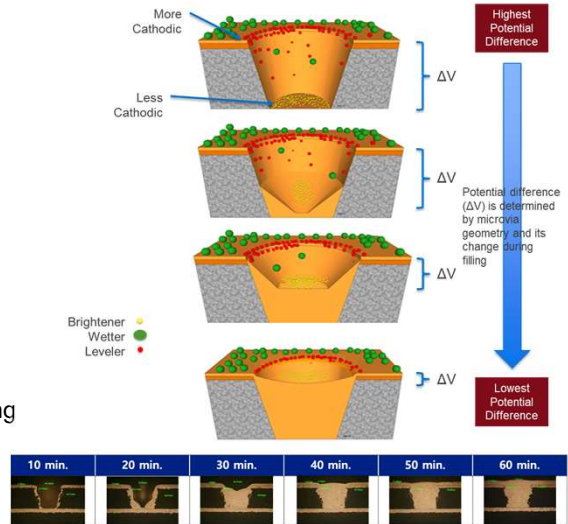
CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

8

Deposition Mechanism

- **Bath composition**
 - Lower H_2SO_4 to reduce solution **conductivity** and promote larger difference in potentials
 - Higher $CuSO_4$ to increase **filling** speed
 - **Chloride** ions provide adsorption **sites**
- **Additives**
 - **Suppressor** preferentially adsorbed on the surface
 - **Brightener** diffuses to the bottom of the microvia
 - **Leveler** selectively adsorbs on the high current areas
- **Fill progression**
 - Plating at via bottom is fastest at the beginning
 - As plating proceeds, the potential differences and plating rate difference of surface and microvia lessen
 - Once filled, all plating rates are similar

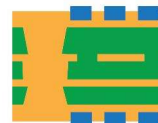
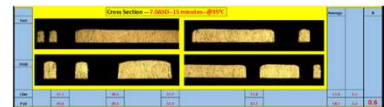
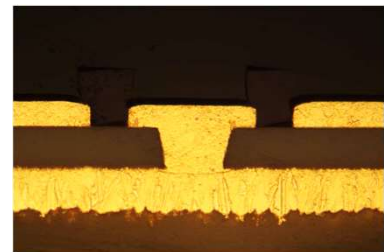


CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions 9

System UVF 200 Process Overview

- DC Acid Copper plating process specifically designed for **2-in-1 RDL applications for FCBGA**
 - **Pattern plate process**
 - **High coplanarity of traces and pads**
 - Typically, $<2 \mu m$ R-Value
 - **Highly controlled trace profile**
 - Typically, $<15\%$
 - **Via Fill**
 - Up to $60 \mu m \varnothing \times 30-35 \mu m$ deep
 - Dimple: $<5 \mu m$, Overfill $<3 \mu m$
 - Surface Copper: $10-15 \mu m$
- **Compatible with High-Speed Plating Tools**
 - ASM-NEXX Stratus P500
 - Semsysco



Imaging Electroplating



Strip Final Etch



CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions 10

Process Cycle and Operating Parameters



Cleaner	Chemistry	Concentration
Additive	Acid Cleaner	10%
	H ₂ SO ₄	5%
Parameter	Dwell time	1-5 min
	Temp	20-35°C

Acid Dip	Chemistry	Concentration
Additive	H ₂ SO ₄	5-10%
Parameter	Dwell time	1 min
	Temp	20-25°C

Bath Make-up

UVF	Chemistry	Concentration
VMS	CuSO ₄	230 g/L
	H ₂ SO ₄	120 g/L
	Cl ⁻	50 ppm
Additives	Leveler	5 ml/L
	Brightener	2 ml/L
	Wetter	10 ml/L
Parameter	CD	1.0-7.0 ASD
	Temp	30-35°C



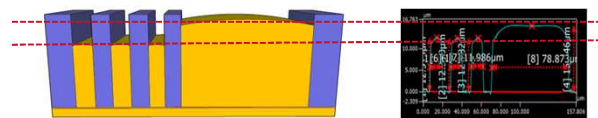
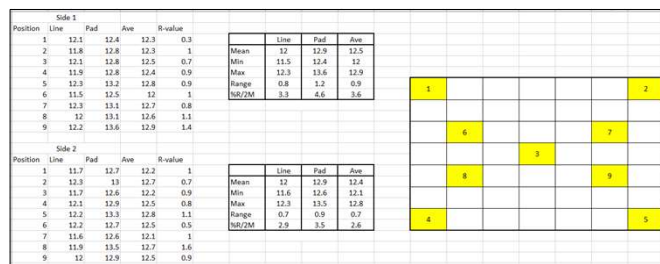
CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

Capabilities

- Panels with different designs, feature sizes, and copper thickness specifications were plated during the evaluation

Features/Spec	Design 1	Design 2
Line/Space	9/12 μm	15/20 μm
BMV Diameter	40 μm	49 μm
BMV Depth	15 μm	20 μm
Plating Thickness	12 μm	17 μm
Plating Time	15 minutes	15 minutes
Current Density	4-5 ASD	5-6 ASD
Dimple	± 2 μm ± 2 μm (POR)	± 2 μm + 2 μm (POR)
Uniformity (WIU)	2 μm 4 μm (POR)	<5 μm 8 μm (POR)
Uniformity (WIP)	<15% 20% (POR)	<15% 20% (POR)
Anode	Insoluble	Insoluble



- 9 areas were measured on each side of the panel
- The best result was with 200/120/50 VMS

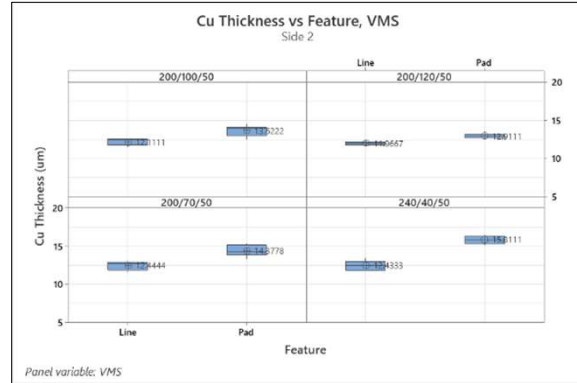
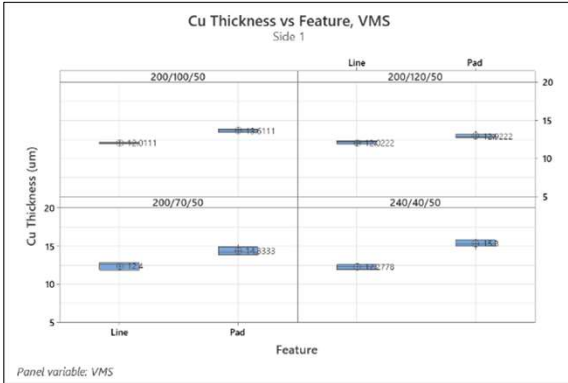


CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

Substrate Design 1 Results

Copper Thickness vs Feature, VMS



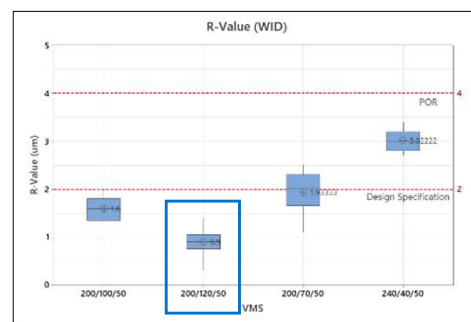
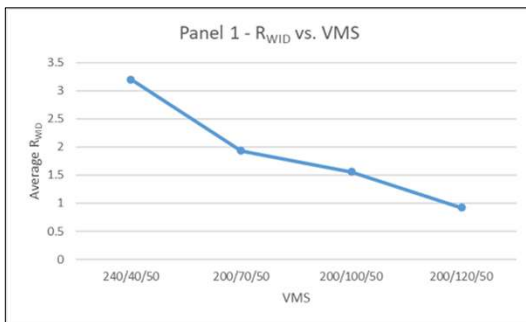
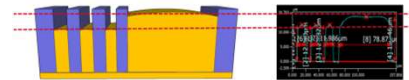
CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

13

Substrate Design 1

Uniformity



- The average R_{WID} was calculated via the difference on the plated height between fine line and pad/filled via
- **R-value improved with lower copper sulfate and higher sulfuric acid**
- **WID uniformity was < 2 um with copper sulfate concentration < 200 g/L**
- **WID uniformity was further improved with additional sulfuric acid**



CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

14

Capabilities

- Panels with different designs, feature sizes, and copper thickness specifications were plated during the evaluation

Features/Spec	Example 1	Example 2
Line/Space	9/12 μm	15/20 μm
BMV Diameter	40 μm	49 μm
BMV Depth	15 μm	20 μm
Plating Thickness	12 μm	17 μm
Plating Time	15 minutes	15 minutes
Current Density	4-5 ASD	5-6 ASD
Dimple	$\pm 2 \mu\text{m}$ $\pm 2 \mu\text{m}$ (POR)	$\pm 2 \mu\text{m}$ $+ 2 \mu\text{m}$ (POR)
Uniformity (WIU)	2 μm 4 μm (POR)	<5 μm 8 μm (POR)
Uniformity (WIP)	<15% 20% (POR)	<15% 20% (POR)
Anode	Insoluble	Insoluble

Side 1				
Position	Line	Pad	Ave	R-value
1	12.1	12.4	12.3	0.3
2	11.8	12.8	12.3	1
3	12.1	12.8	12.5	0.7
4	11.9	12.8	12.4	0.9
5	12.3	13.2	12.8	0.9
6	11.5	12.5	12	1
7	12.3	13.1	12.7	0.8
8	12	13.1	12.6	1.1
9	12.2	13.6	12.9	1.4

Line	Pad	Ave	
Mean	12	12.9	12.5
Min	11.5	12.4	12
Max	12.3	13.6	12.9
Range	0.8	1.2	0.9
Std/2M	3.3	4.6	3.6

Side 2				
Position	Line	Pad	Ave	R-value
1	11.7	12.7	12.2	1
2	12.3	13	12.7	0.7
3	11.7	12.6	12.2	0.9
4	12.1	12.9	12.5	0.8
5	12.2	13.3	12.8	1.1
6	12.2	12.7	12.5	0.5
7	11.6	12.6	12.1	1
8	11.9	13.5	12.7	1.6
9	12	12.9	12.5	0.9

Line	Pad	Ave	
Mean	12	12.9	12.4
Min	11.6	12.6	12.1
Max	12.3	13.5	12.8
Range	0.7	0.9	0.7
Std/2M	2.9	3.5	2.6

- 9 areas were measured on each side of the panel by ZYGO profiler
- The best result was with 200/120/50 VMS

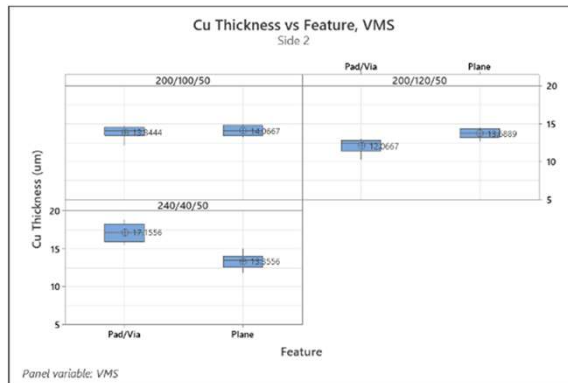
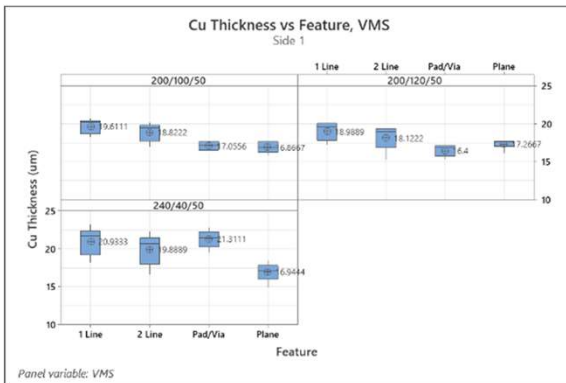


CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

Substrate Design 2 Results

Copper Thickness vs Feature, VMS

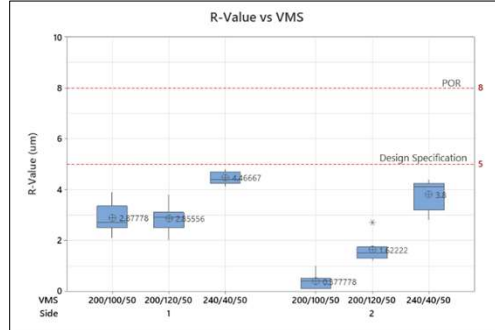
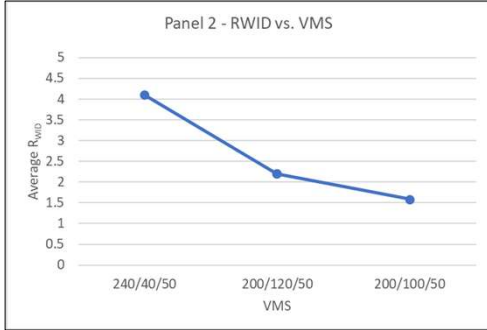
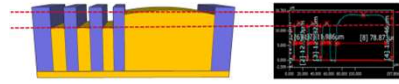


CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

Substrate Design 2 Results

Uniformity



- The average R_{WID} was calculated via the difference on the plated height between fine line and pad/filled via
- **R-value improved with lower copper sulfate and higher sulfuric acid**
- **WID uniformity was < 5 um with copper sulfate concentration < 240 g/L**



CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

Via Fill Results

- Via size: 40x15 μm
- Plated thickness: 12 μm
- All conditions resulted in a bump on the filled vias
- As Cu was reduced and acid was increased, the domes on the filled vias decreased and the uniformity improved (reduced R values)

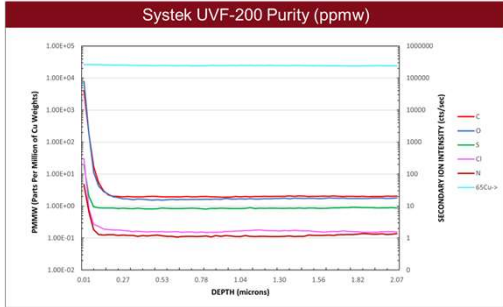
VMS	Bump (μm)
240/40/50	3.8
200/120/50	0.9



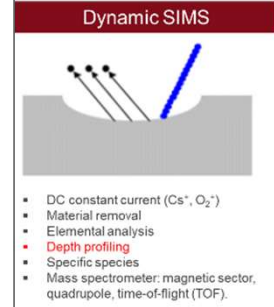
CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

SIMS Analysis



Element	Concentration (ppmw)
Sulfur	0.848
Carbon	1.98
Oxygen	1.66
Chlorine	0.163
Nitrogen	0.114



- Low impurities co deposit with Cu
 - Electrical conductivity, grain structure, Cu reduction during SAP / mSAP, physical properties



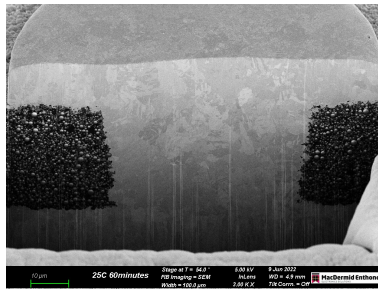
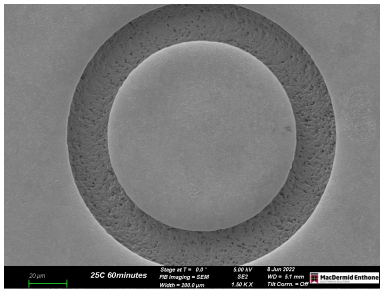
CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

Properties of Deposit

- Physical properties exceeded IPC class III specifications
- Deposit had equiaxial grain structure

Plating Condition	2.0 ASD, 25°C	4.5 ASD, 35°C
Elongation (%)	22.0	20.1
Tensile Strength (kPSI)	40.4	40.4
Internal Tensile Stress (kg/mm ²)	0.87	0.85

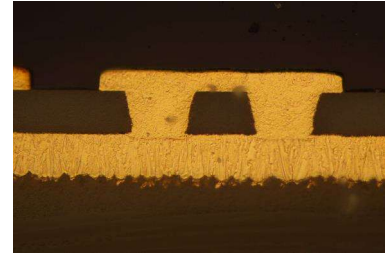


CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions

UVF 200 Summary

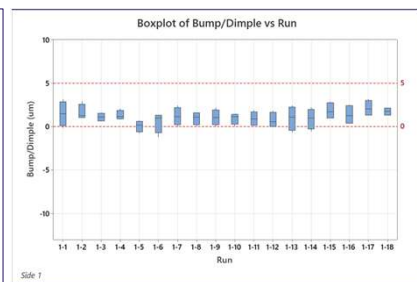
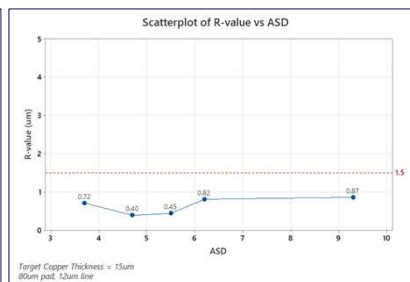
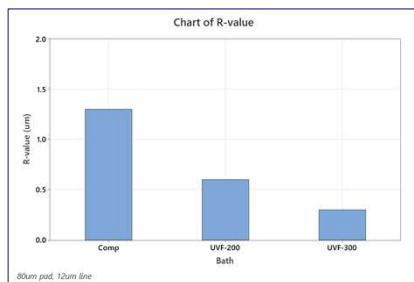
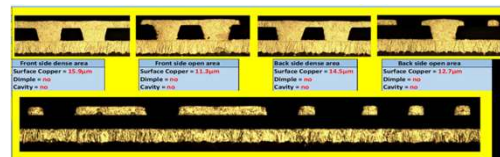
- Systek **UVF 200** is a **versatile** plating process for the **2-in-1 RDL plating** of fine lines and filling of microvias in build up layer applications
 - Filling of microvias **up to 60 μmØ x 30 μmD**
 - Plating **thickness of 15-18 μm** within **15-20 min** plating time
 - **Low R-values** between various features
 - **Good within device (WID) and within panel (WIP) uniformity**
- Process is very stable and tunable
 - **Wide VMS operating range**
 - **Wide operating current density range**
 - Compatible with **Nafion** membranes
 - All additives are **CVS analyzable** and controllable



Next Gen RDL Plating

Systek UVF 300

- Reduced variation in copper thickness
- High coplanarity across a wide range of current density
- Consistent via fill





Contact Us



Sam Dharmarathna

Line of Business Partner – IC substrate R&D

 saminda.dharmarathna@macdermidalpha.com

 macdermidalpha.com

 <https://www.linkedin.com/in/dasaminda/>



CONFIDENTIAL

Circuitry Solutions
Semiconductor & Assembly Solutions
Film & Smart Surface Solutions



CONFIDENTIAL CAUTIONARY STATEMENT

This presentation contains confidential information relating, without limitation, to the Company's products, knowledge, formulations, methods, processes, techniques, suppliers, customers, competition and market shares. This confidential information is strictly private and personal to its recipient and should not be copied, distributed or reproduced in whole or in part, nor communicated to any third party. Recipient shall maintain this confidential information in the strictest secrecy and confidence, with the same degree of care with which it protects its confidential information of like nature, and shall not use this confidential information for any purpose other than the intended purpose discussed with the Company. In addition, industry, market and competitive position data in this presentation are derived from the Company's own internal estimates and research, but also from industry and general publications and research, surveys and studies conducted by third parties. While the Company believes this data is reliable, it has not been verified by any independent source, and as a result, the recipient is cautioned not to place undue reliance on this data.

macdermidalpha.com