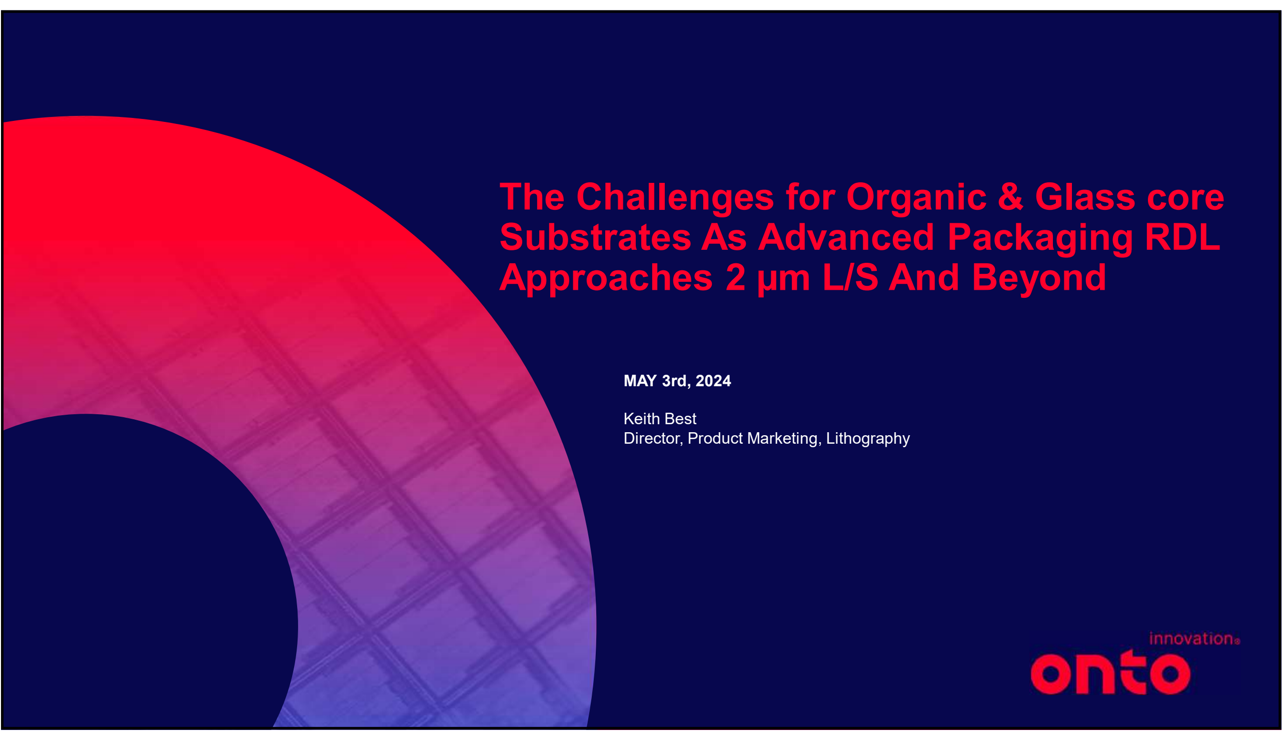

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Disclaimer

Onto Innovation's statements regarding its plans, directions, and intent are subject to change or withdrawal without notice at Onto's sole discretion.

Information regarding potential future products is intended to outline our general product direction and it should not be relied on in making a purchasing decision.

The information mentioned regarding potential future products is not a commitment, promise, or legal obligation to deliver any material, code or functionality. Information about potential future products may not be incorporated into any contract.

The development, release, and timing of any future features or functionality described for our products remains at our sole discretion.

Performance is based on measurements and projections using standard Onto benchmarks in a controlled environment. The actual throughput or performance that any user will experience will vary depending upon many factors. Therefore, no assurance can be given that an individual user will achieve results similar to those stated here.

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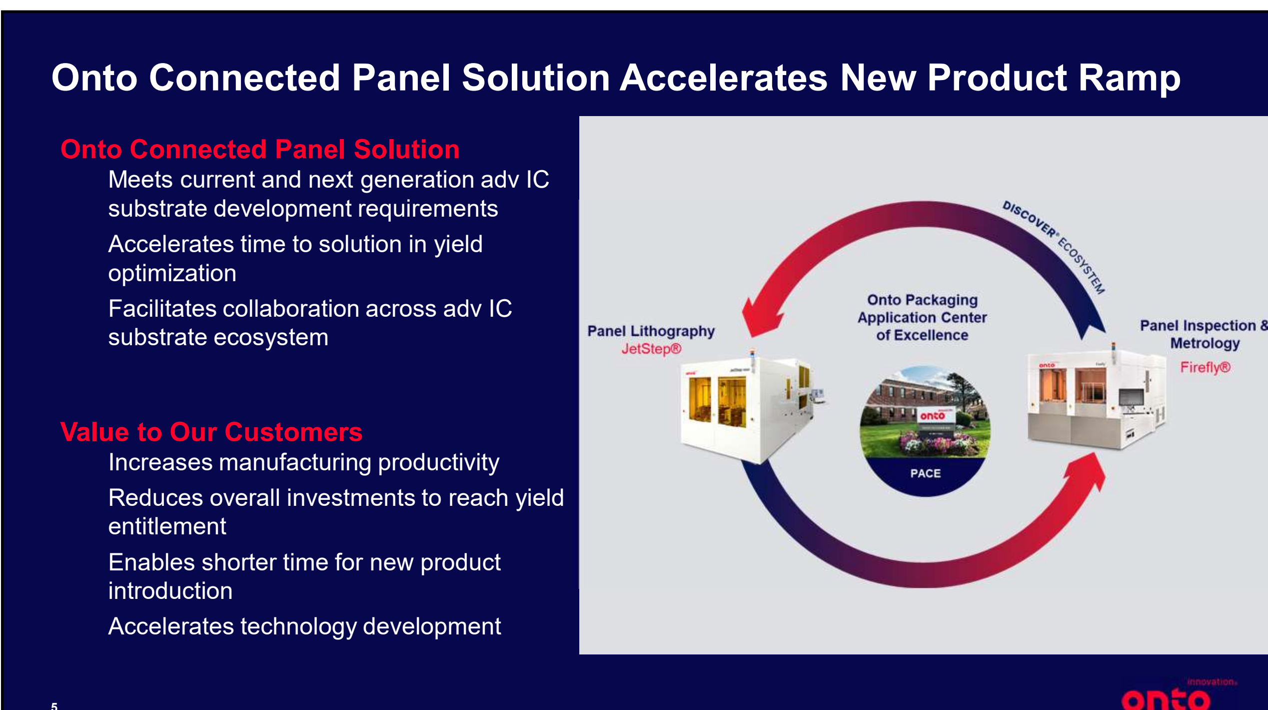

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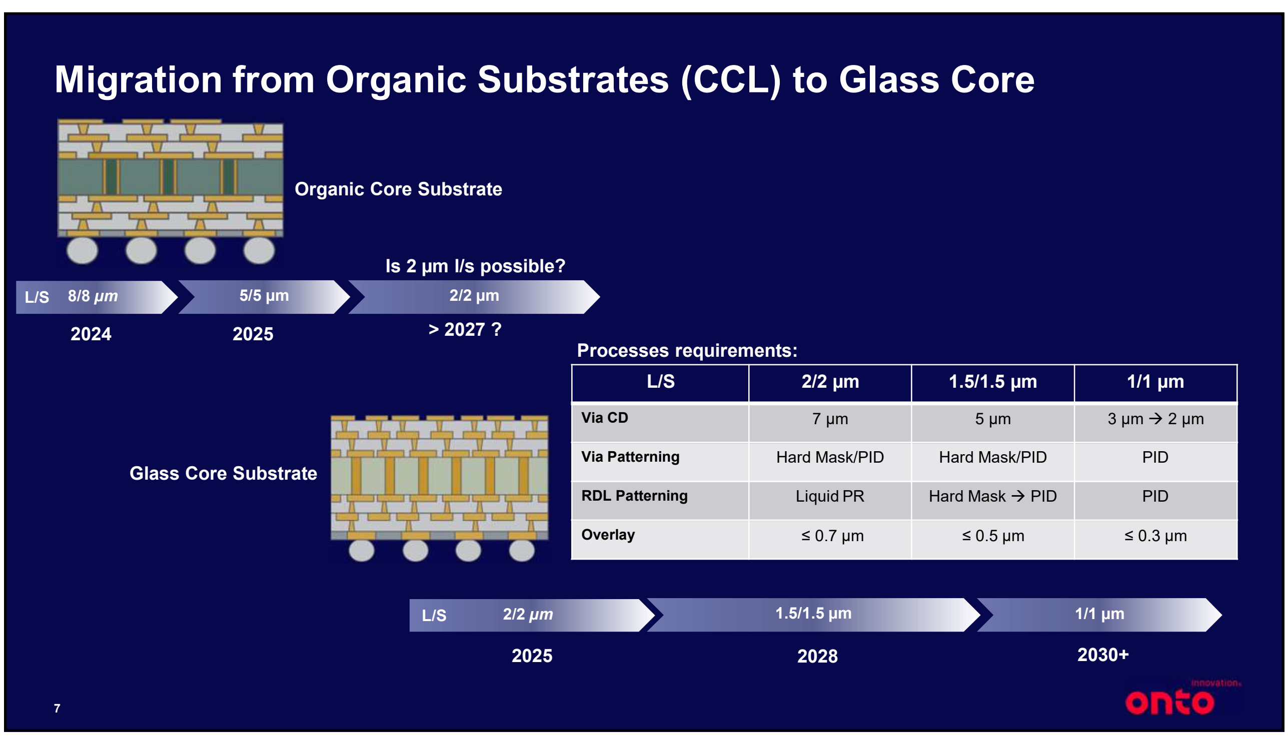

L/S	2/2 µm	1.5/1.5 µm	1/1 µm
Via CD	7 µm	5 µm	3 µm → 2 µm
Via Patterning	Hard Mask/PID	Hard Mask/PID	PID
RDL Patterning	Liquid PR	Hard Mask → PID	PID
Overlay	≤ 0.7 µm	≤ 0.5 µm	≤ 0.3 µm

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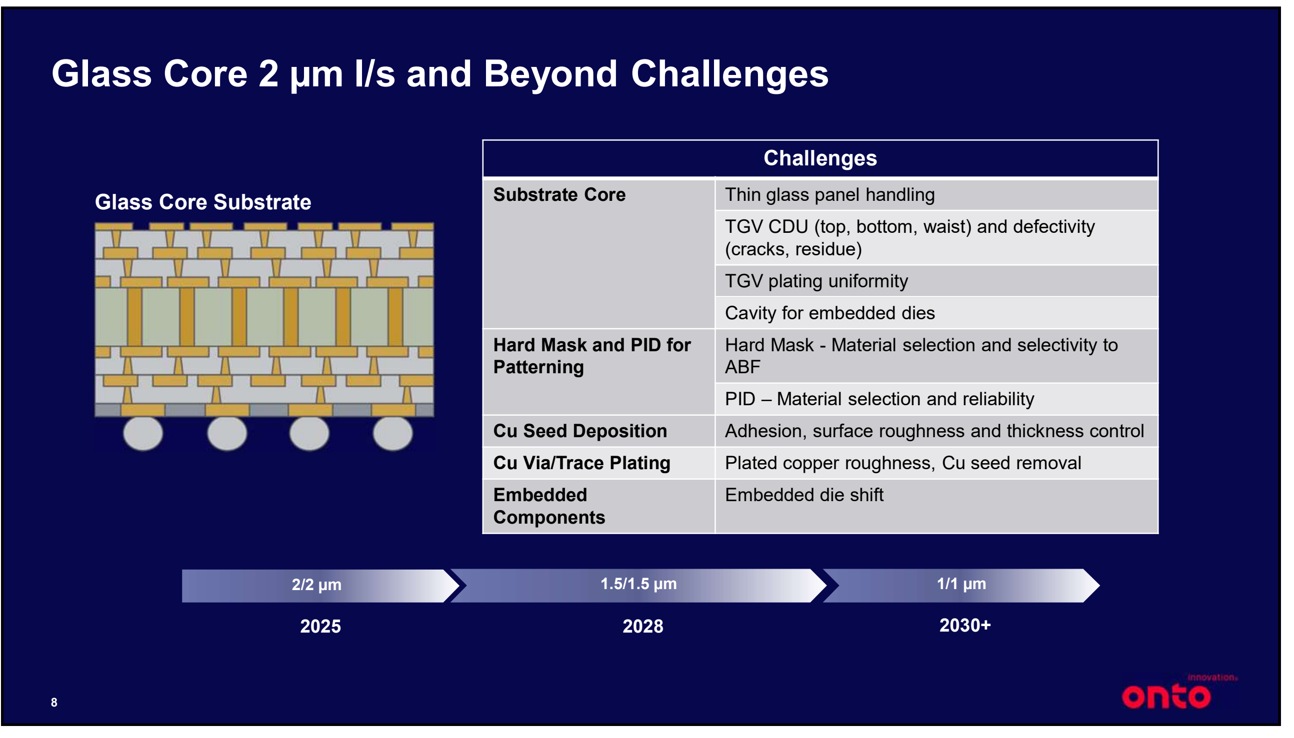
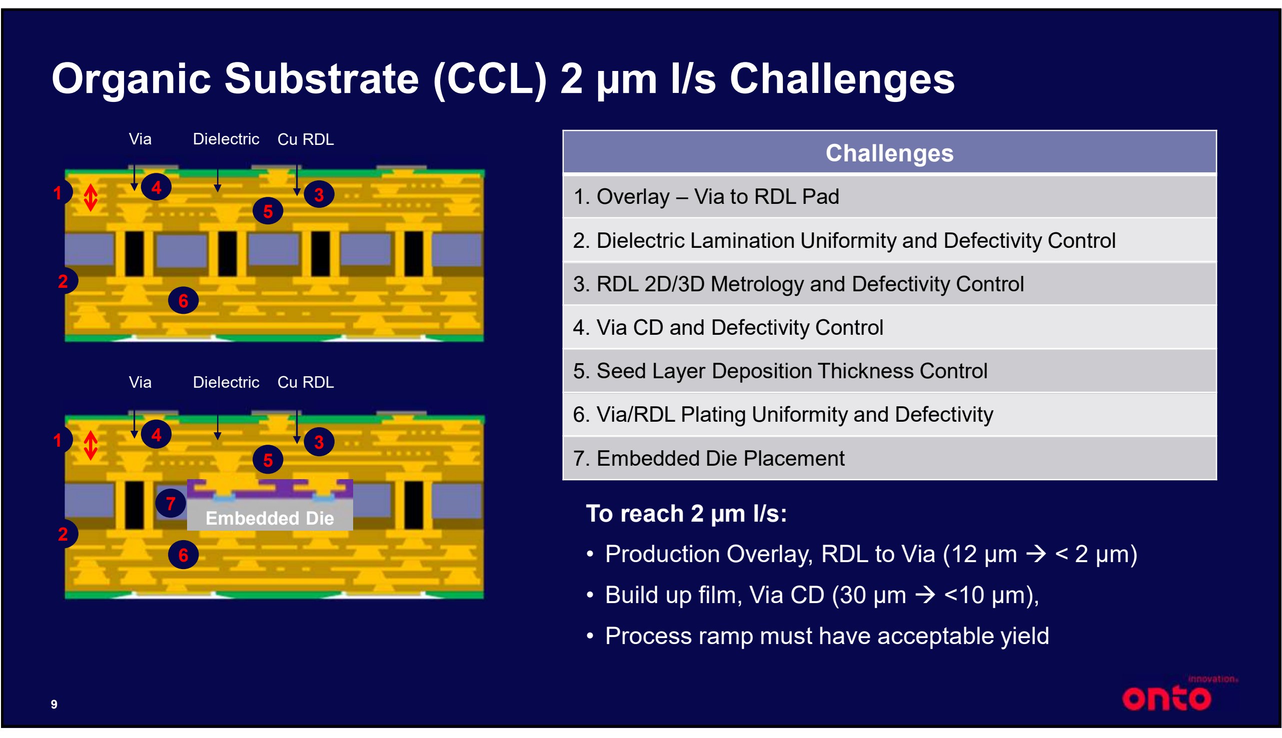


Challenges	
Substrate Core	Thin glass panel handling
	TGV CDU (top, bottom, waist) and defectivity (cracks, residue)
	TGV plating uniformity
	Cavity for embedded dies
Hard Mask and PID for Patterning	Hard Mask - Material selection and selectivity to ABF
	PID – Material selection and reliability
Cu Seed Deposition	Adhesion, surface roughness and thickness control
Cu Via/Trace Plating	Plated copper roughness, Cu seed removal
Embedded Components	Embedded die shift

8



9

Organic Substrate (CCL) 2 µm l/s Challenges

Via | Dielectric | Cu RDL

Embedded Die

Challenges
1. Overlay – Via to RDL Pad
2. Dielectric Lamination Uniformity and Defectivity Control
3. RDL 2D/3D Metrology and Defectivity Control
4. Via CD and Defectivity Control
5. Seed Layer Deposition Thickness Control
6. Via/RDL Plating Uniformity and Defectivity
7. Embedded Die Placement

To reach 2 µm l/s:

- Production Overlay, RDL to Via (12 µm → < 2 µm)
- Build up film, Via CD (30 µm → <10 µm),
- Process ramp must have acceptable yield

10

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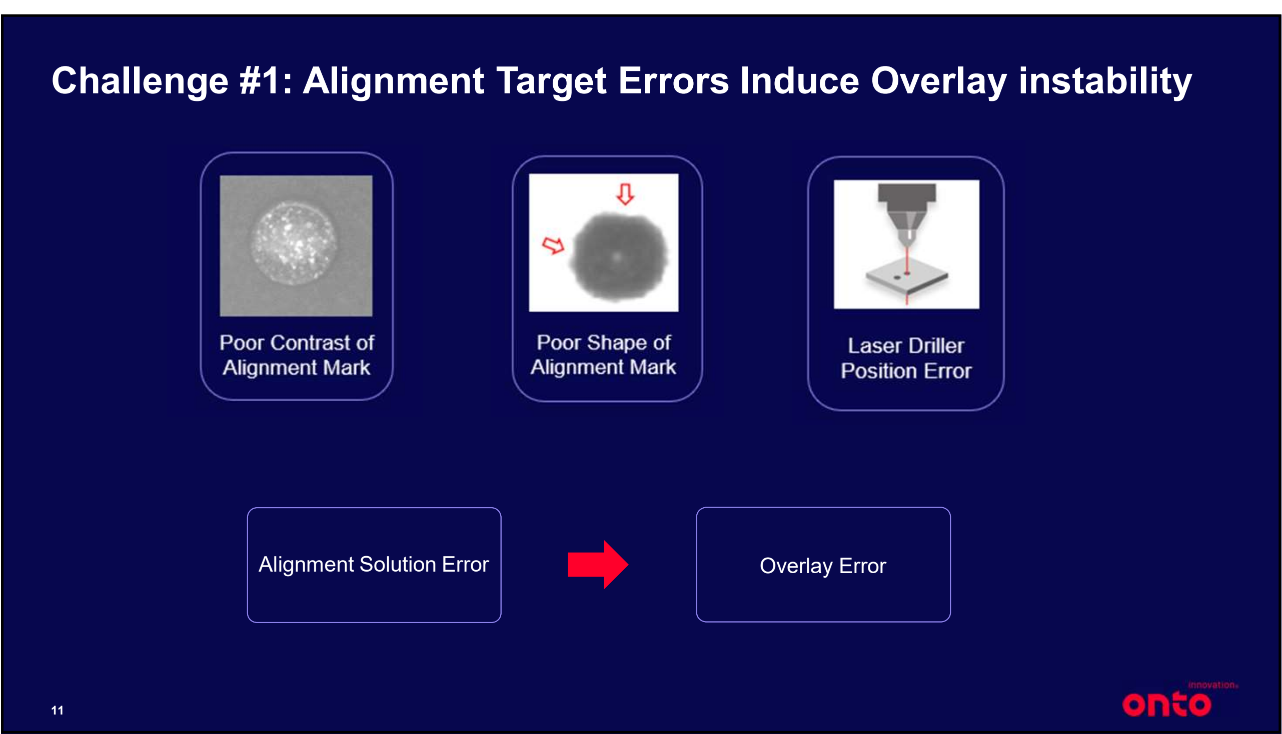

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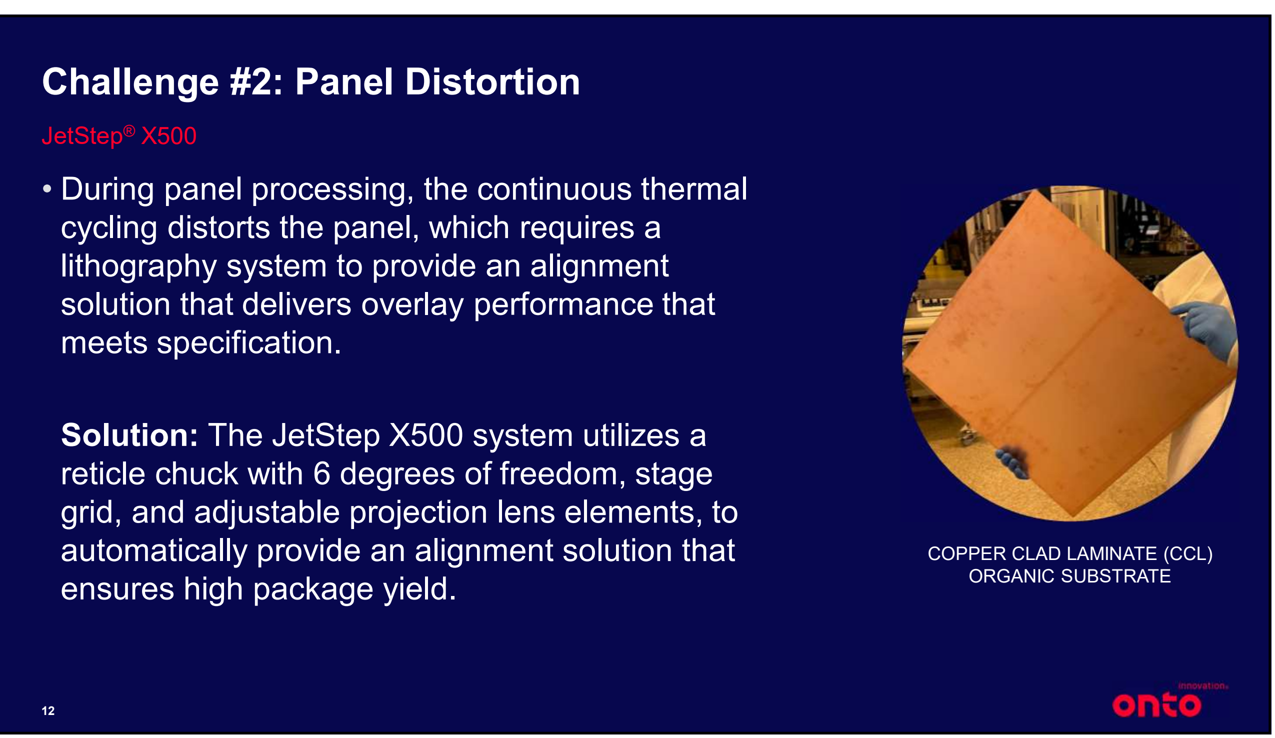

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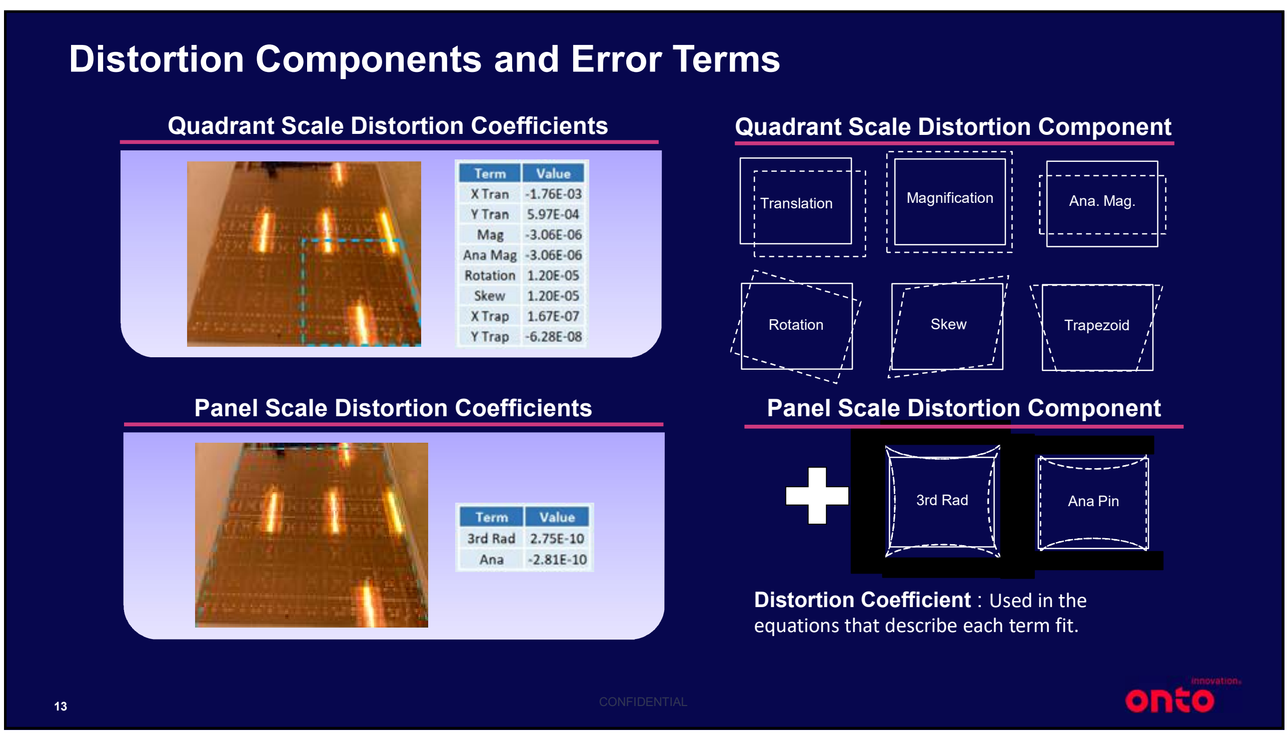

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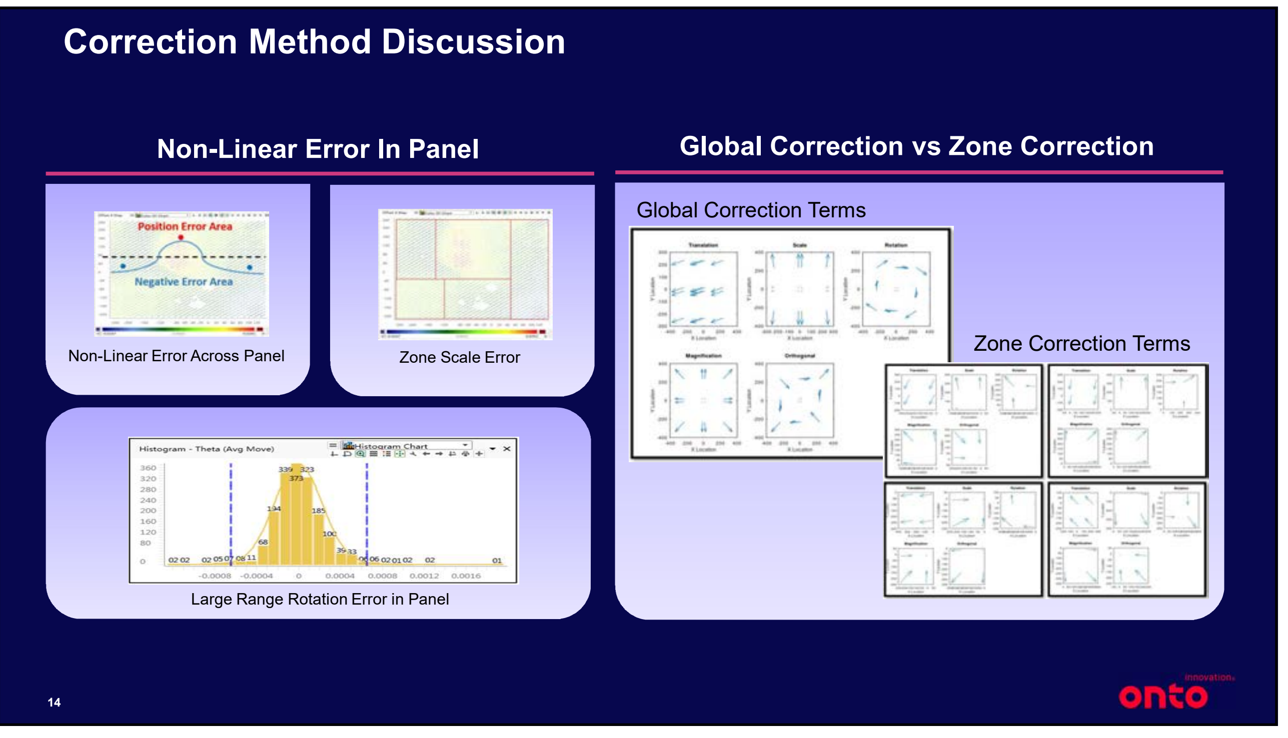

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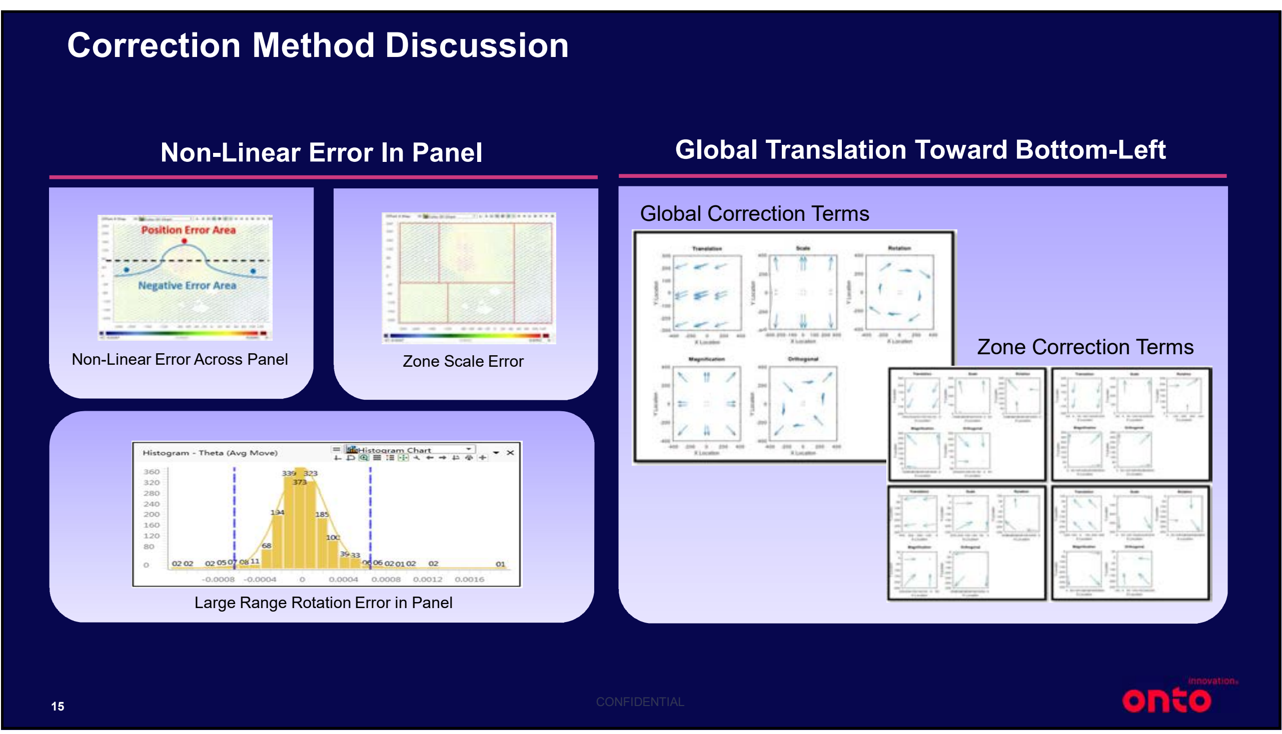

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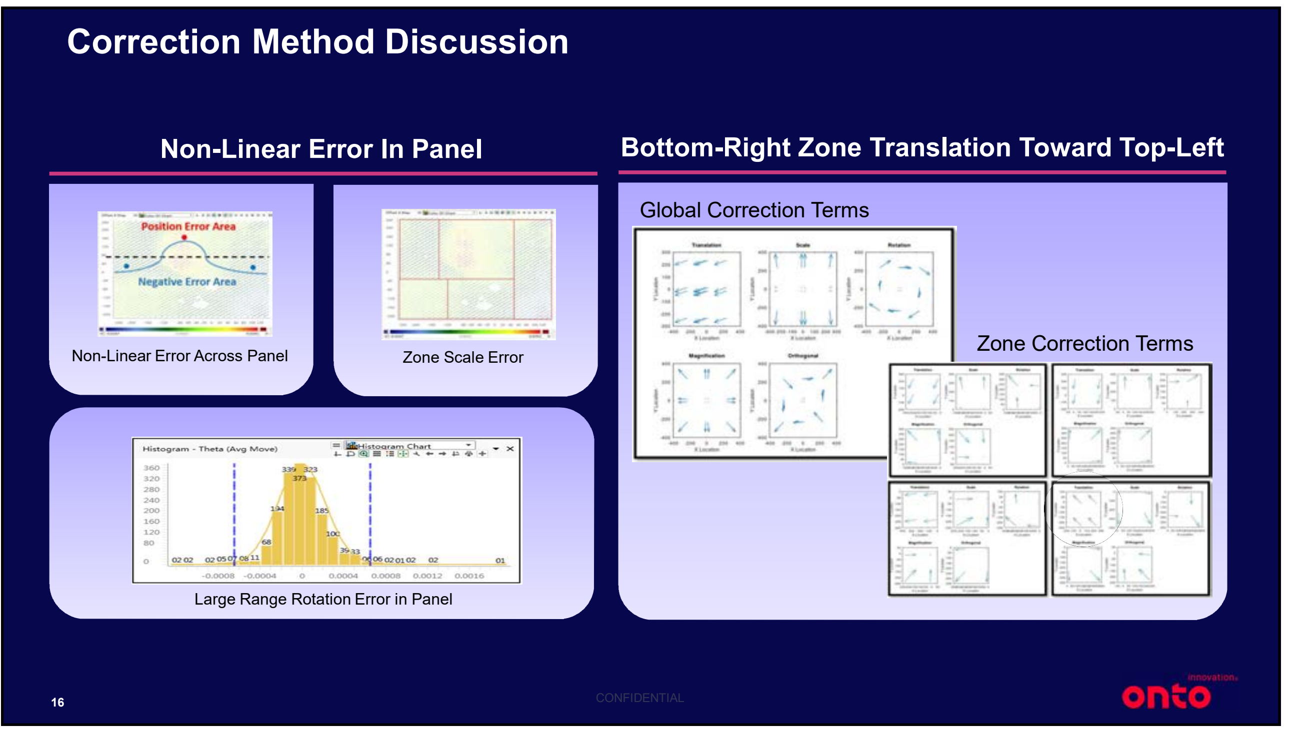

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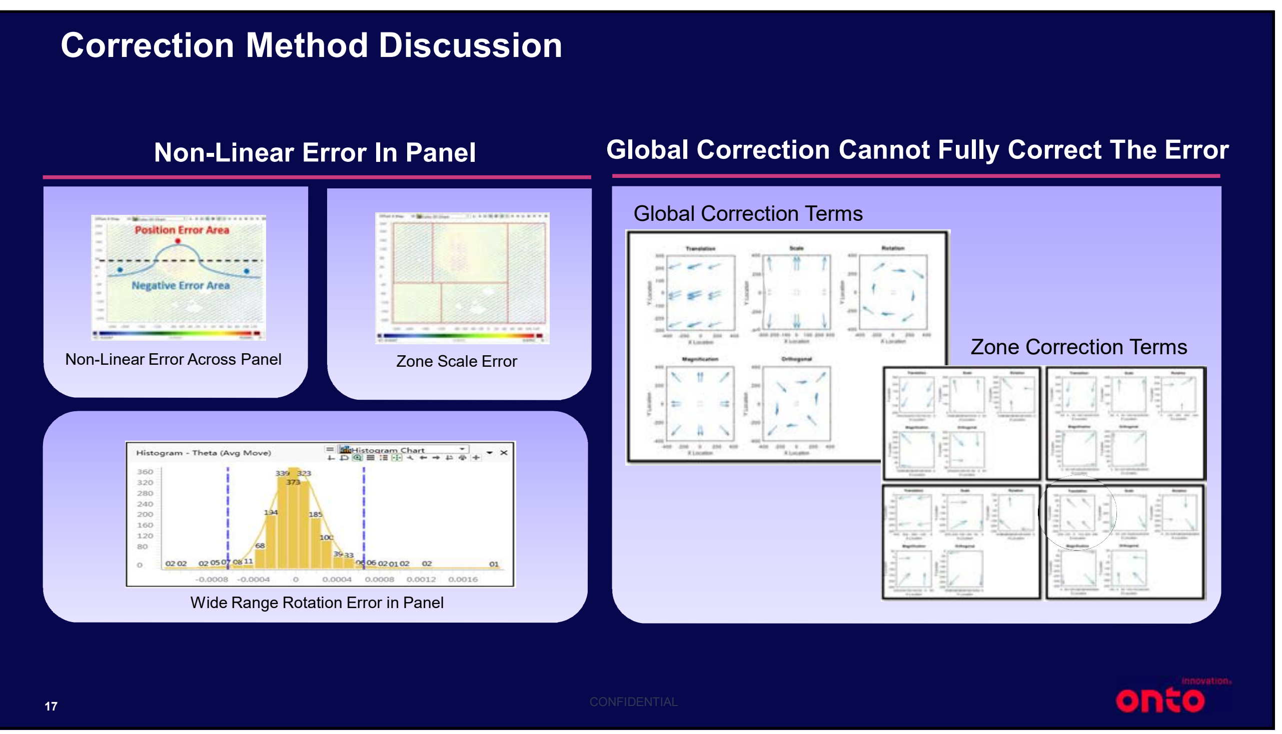

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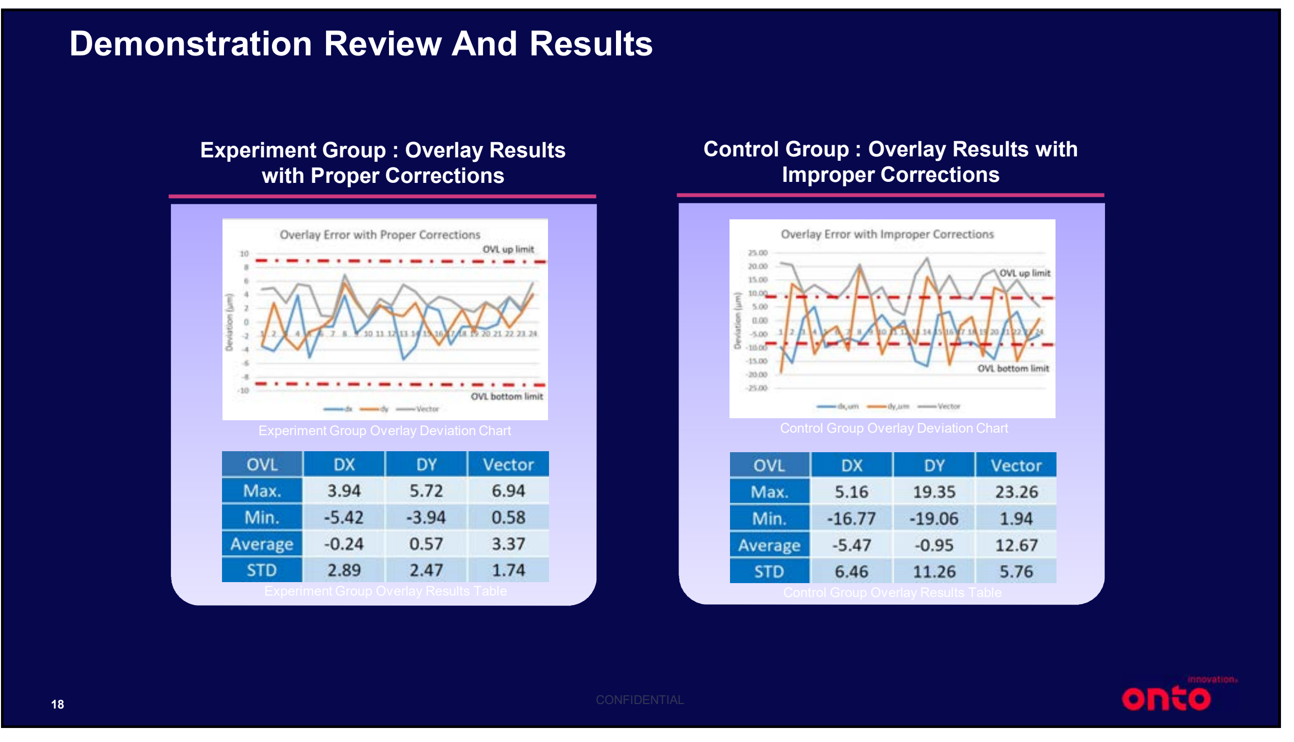


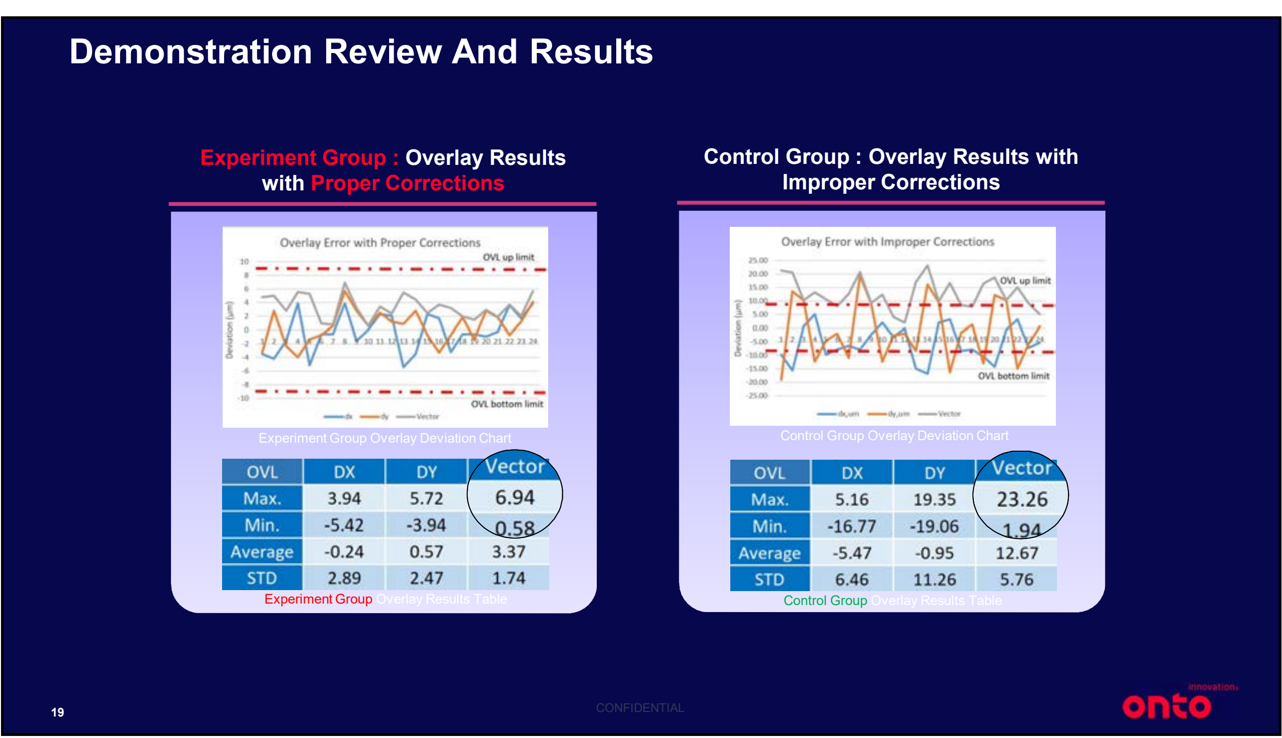
OVL	DX	DY	Vector
Max.	3.94	5.72	6.94
Min.	-5.42	-3.94	0.58
Average	-0.24	0.57	3.37
STD	2.89	2.47	1.74

Experiment Group Overlay Results Table

OVL	DX	DY	Vector
Max.	5.16	19.35	23.26
Min.	-16.77	-19.06	1.94
Average	-5.47	-0.95	12.67
STD	6.46	11.26	5.76

Control Group Overlay Results Table

18



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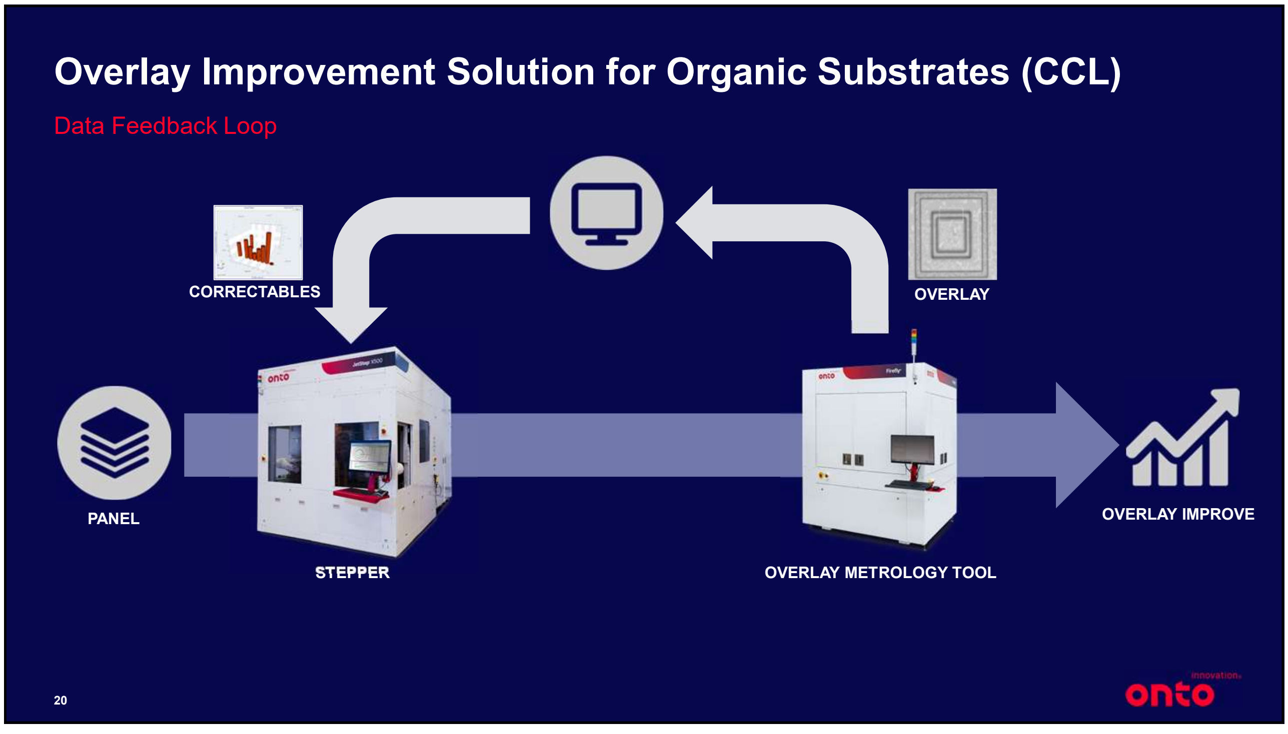

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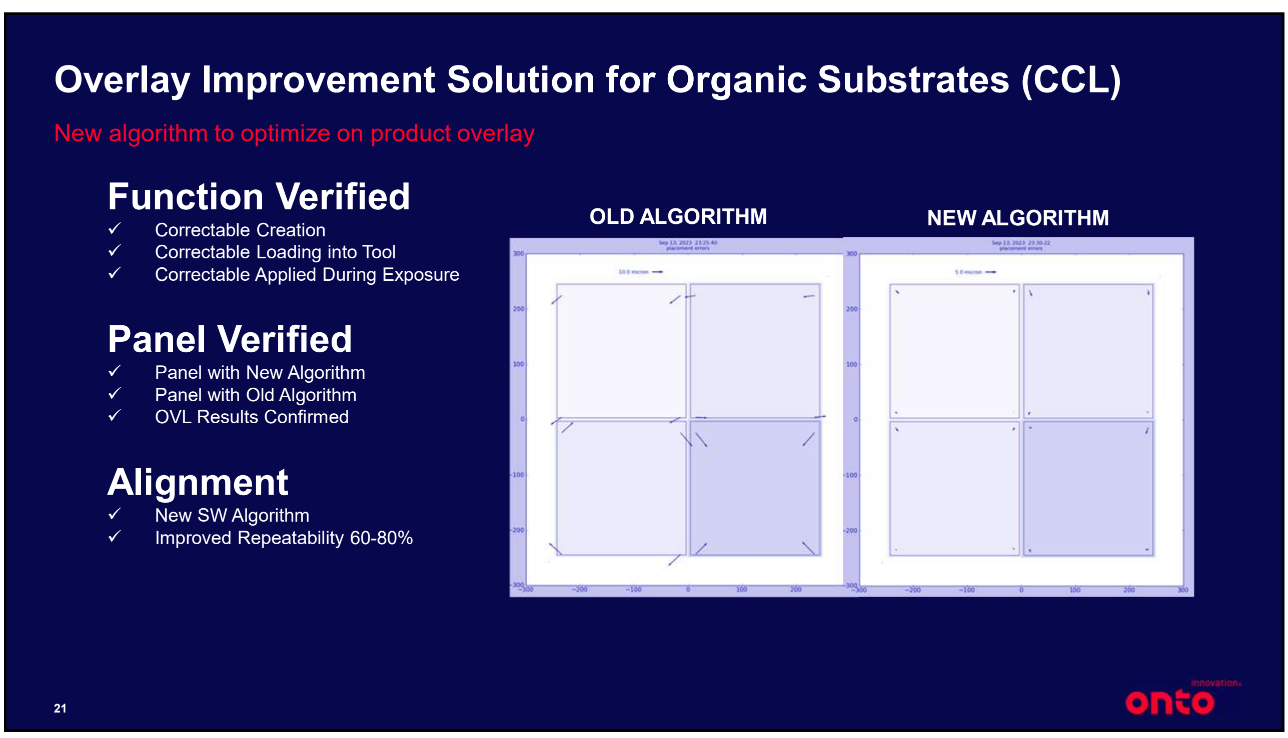

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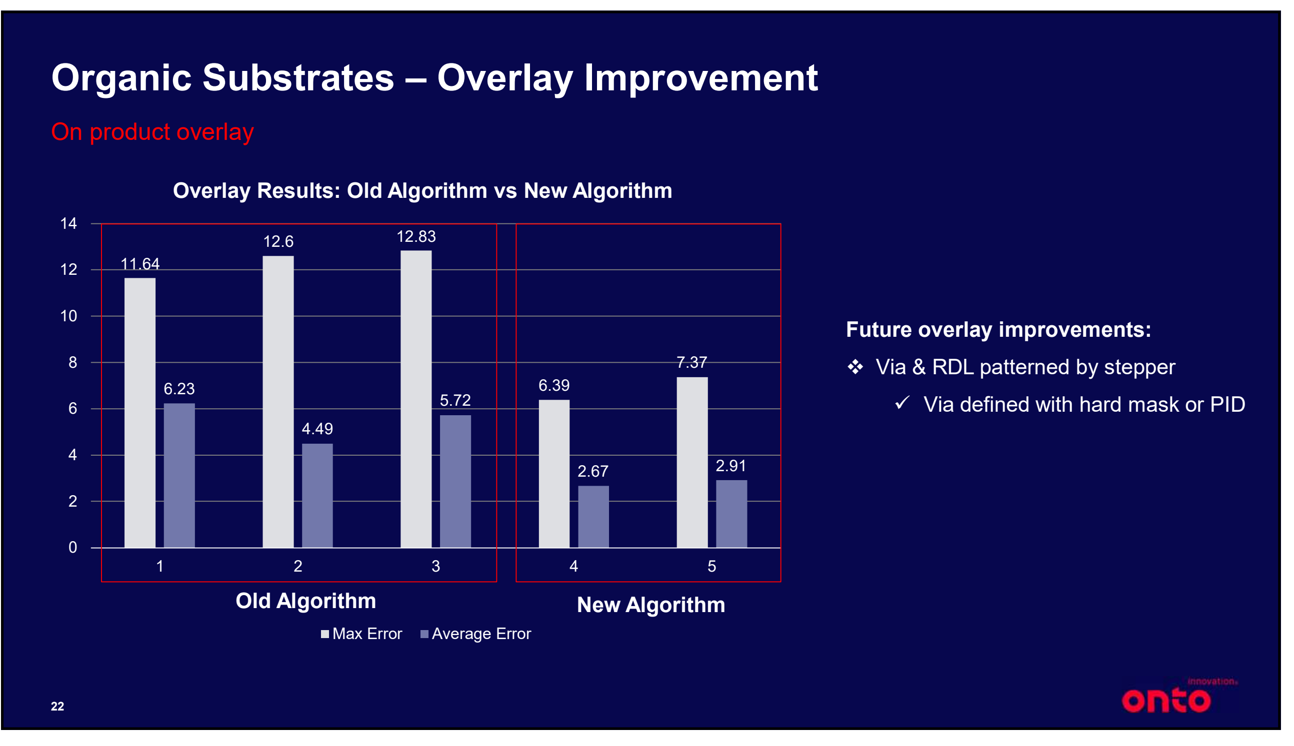

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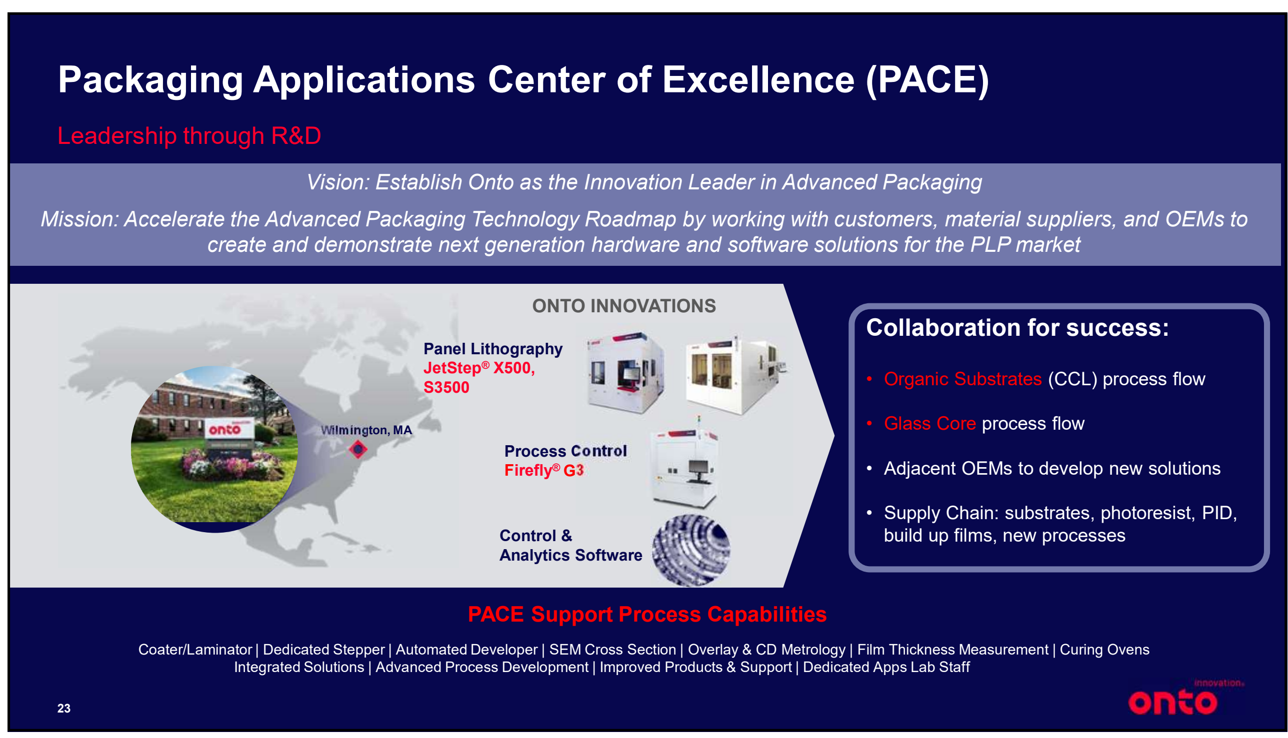

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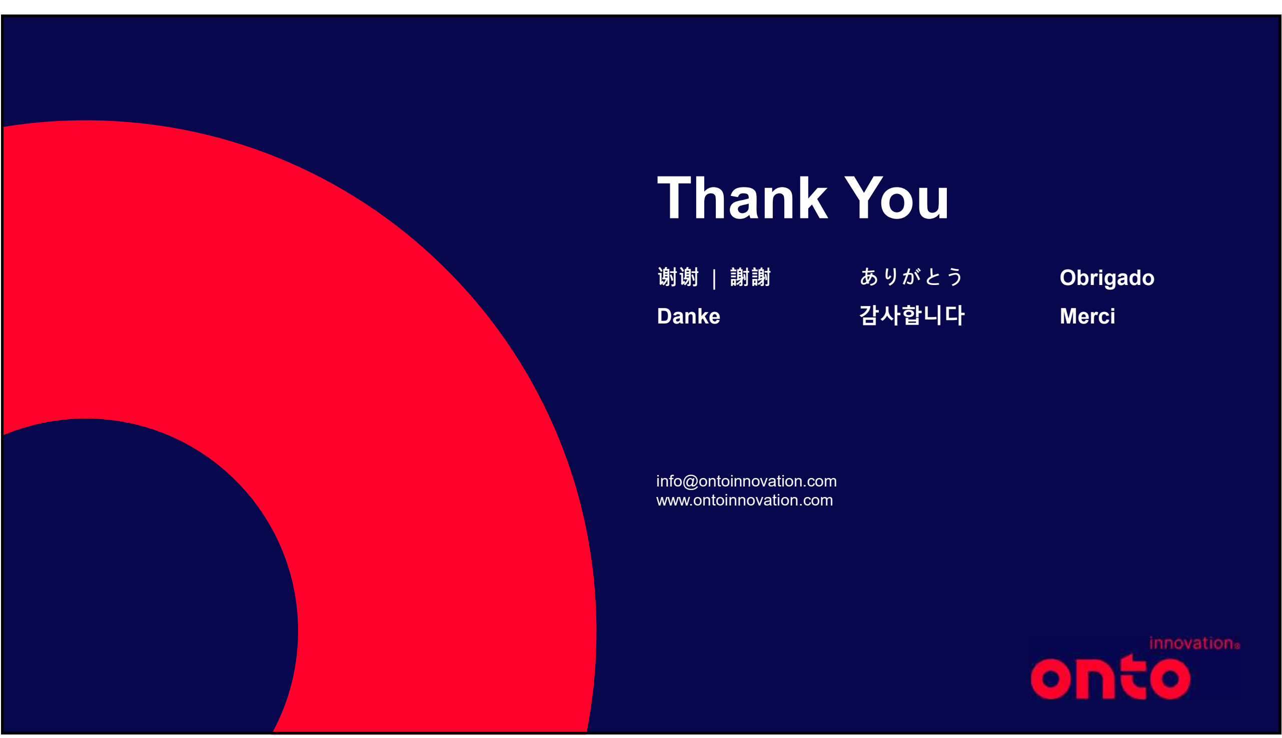

24

Abstract: *"As the Advanced Packaging substrate interconnect density continues to increase rapidly, driven by next generation HPC, AI and VR/AR applications, there has been a paradigm shift in the package architecture to replace organic substrates with glass core substrates. Typically, organic substrates support HVM RDL structures of 9/12 μm line/space and, in R&D, down to 5/5 μm line/space. Beyond this, the substrate's dimensional stability and flatness will limit the resolution and overlay performance, impacting customer product roadmaps. Glass core substrates are expected to provide the solution. However, glass core has its own challenges. Onto Innovation understands these challenges, and provides solutions through its lithography, inspection, metrology and SW products. Onto Innovation is working with adjacent OEMs and the material supply chain to provide customers with early access to next generation products through its Packaging Applications Center of Excellence (PACE). This talk will discuss the benefits and challenges of both architectures and explores the possibility of extending the useful life of organic substrates beyond 5/5 μm line/space.*

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