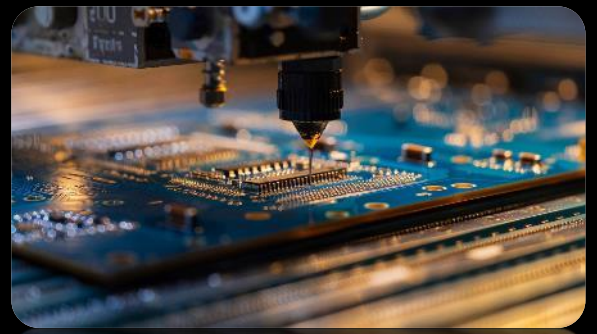
The Future of AI and HPC Substrates: A Breakthrough Interconnect Technology

Rozalia Beica – Chief Commercial Officer

Build-Up Substrate Symposium | May 2-3, 2024

Presentation Agenda

Industry Trends



- Semiconductor Industry
- Information Age / AI & HPC

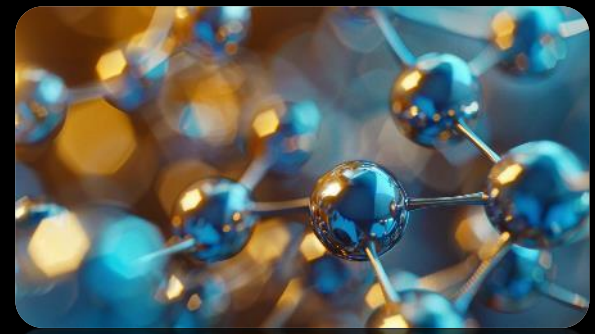
Current Challenges

- Increased Complexity
- High Density Interconnects

LQDX Introduction

- Introduction
- Technology

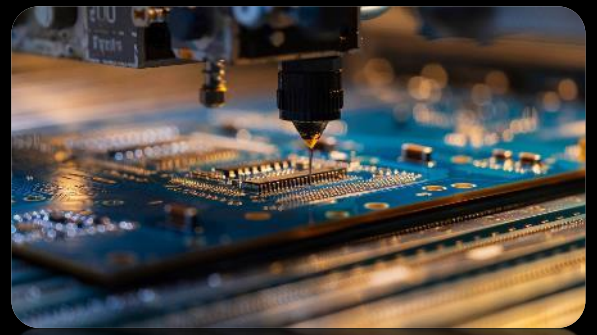
Our Solutions



- High Density Interconnects
- The Road to 1um

Presentation Agenda

Industry Trends



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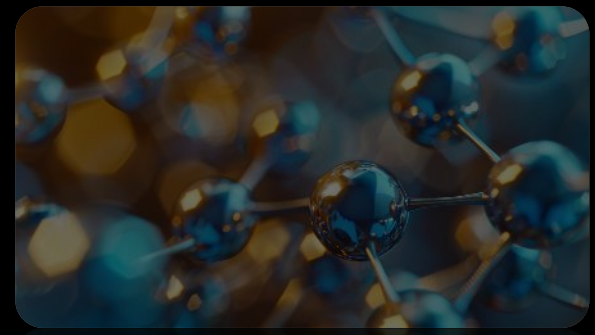

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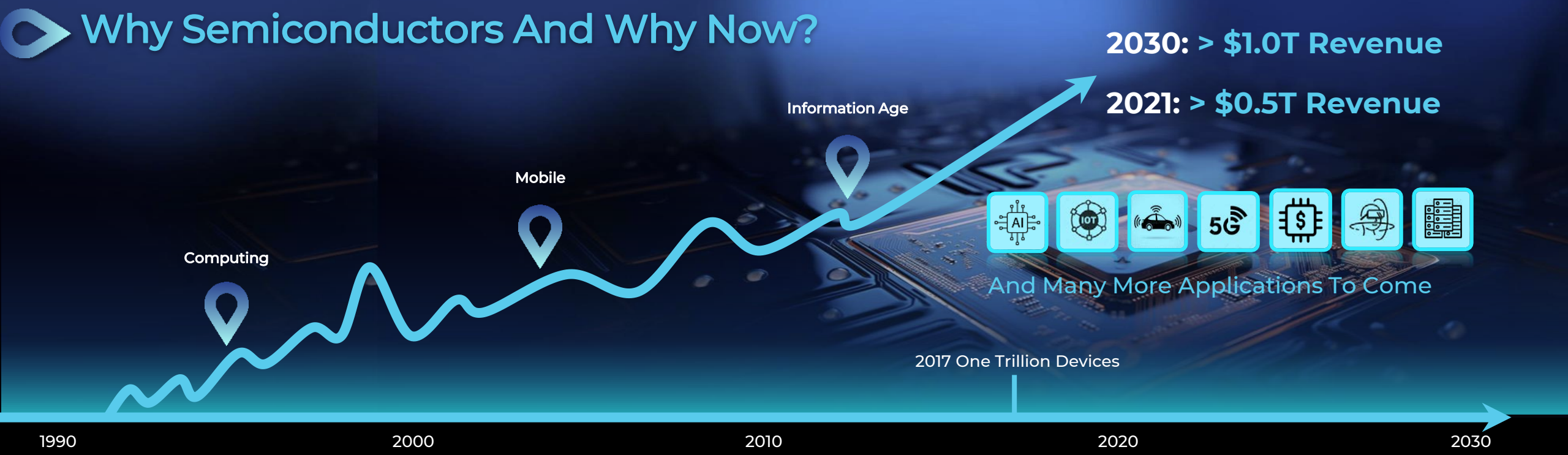
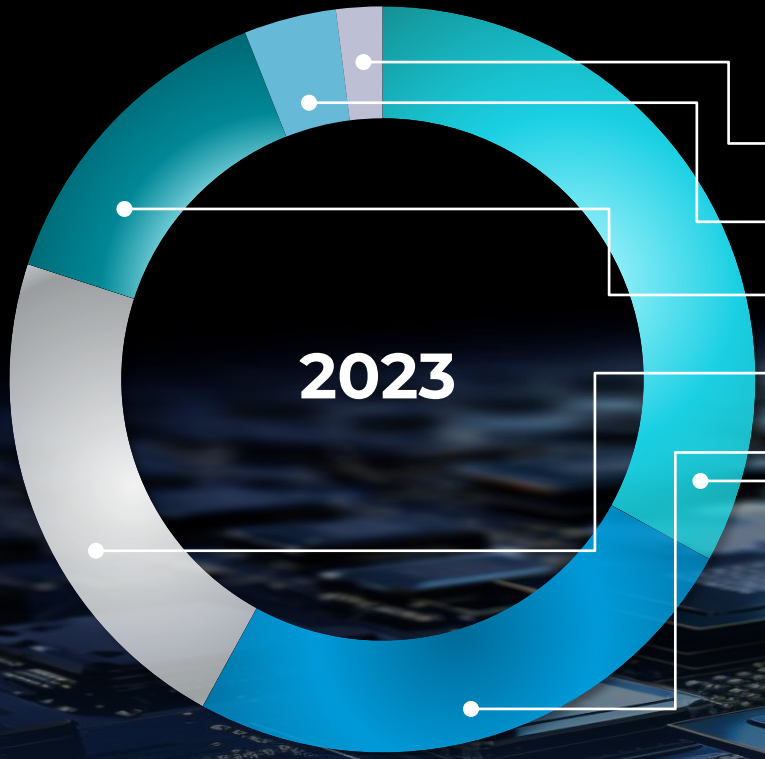
Why Semiconductors And Why Now?



The semiconductor industry has never seen anything like this at any time in its history!

- In the past, there was always One Key Technology driving the roadmap: e.g. PC -> Mobile -> Smartphone -> Information Age
- Now there are multiple growth technologies ramping at the same time: AI, 5G, Datacenter, VR/AR, IIoT, Autonomous Driving, etc.
- AI & HPC are driving an unprecedented market inflection, and many processes and materials are needed to satisfy the demand
- All of this also being catalyzed by government investments worldwide

AI And HPC: The Next Growth Engine For Semiconductors



Semiconductor Market By Applications

- **02%** - IOT / Edge Compute
- **04%** - Autonomous Driving
- **14%** - Mobile Advertising
- **22%** - Network / Datacenter
- **25%** - Consumer / AVR / VR
- **33%** - HPC / AI

Source: Semiconductor End-Market Driver Breakdown By End Application, McKinsey 2023

HPC / AI – ALREADY THE DOMINANT APPLICATION DRIVING THE GROWTH OF OUR INDUSTRY

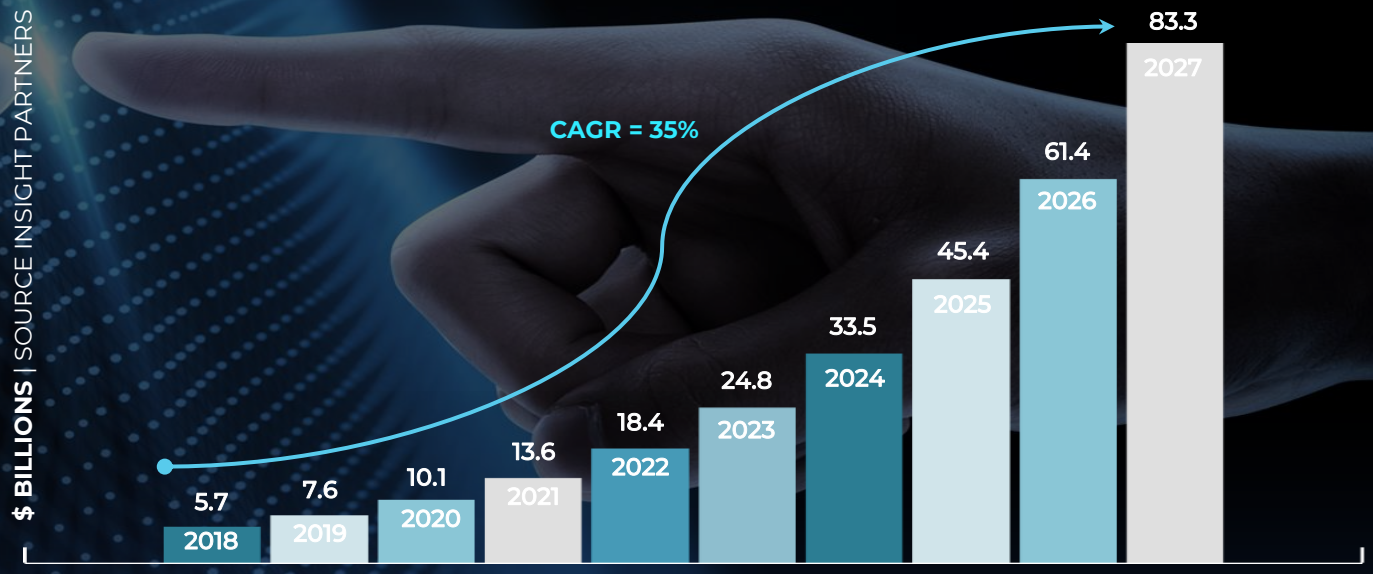
AI: Catalyzing The Next Growth Wave Of Semiconductors

Wide Range Of Applications

- Deep Learning
- Machine Learning
- Simulation / Modeling
- Natural Language Processing
- Image Analytics
- Graph Analytics
- Robotics / Automation
- Autonomous Vehicles
- Healthcare
- IoT
- ----

Generative AI: similar impact to that of the steam engine, electricity & the internet

Source: Gartner



10X Higher Growth Rate for AI Chips vs Non-AI

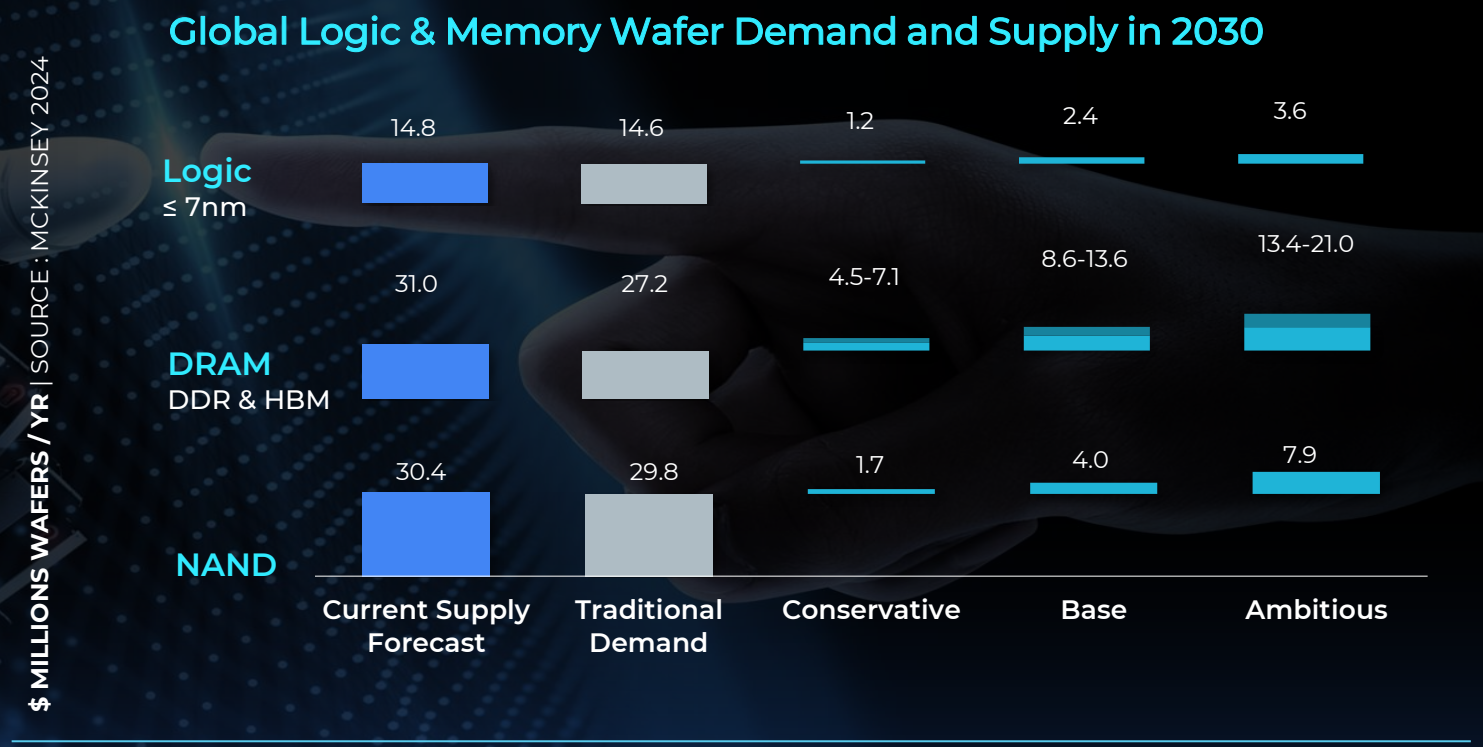
Can The Industry Keep Up With The Growth Of Generative AI?

Logic

- 2030 (non-AI) demand: 15M wafers
- 2030 fab planning / supply: 15M wafers
- 2030 gen. AI demand: + 1.2 – 3.6M wafers
- Supply Gap due to Gen. AI: 1-4M wafers

Memory

- Memory capacity & bandwidth bottlenecks
- The growth in memory capacity is not straightforward, posing challenges to hardware and software design
- New memories being tested for near-compute memory – high cost limits adoption



To Close the Gap, 3-9 New Logic Fabs will be needed by 2030

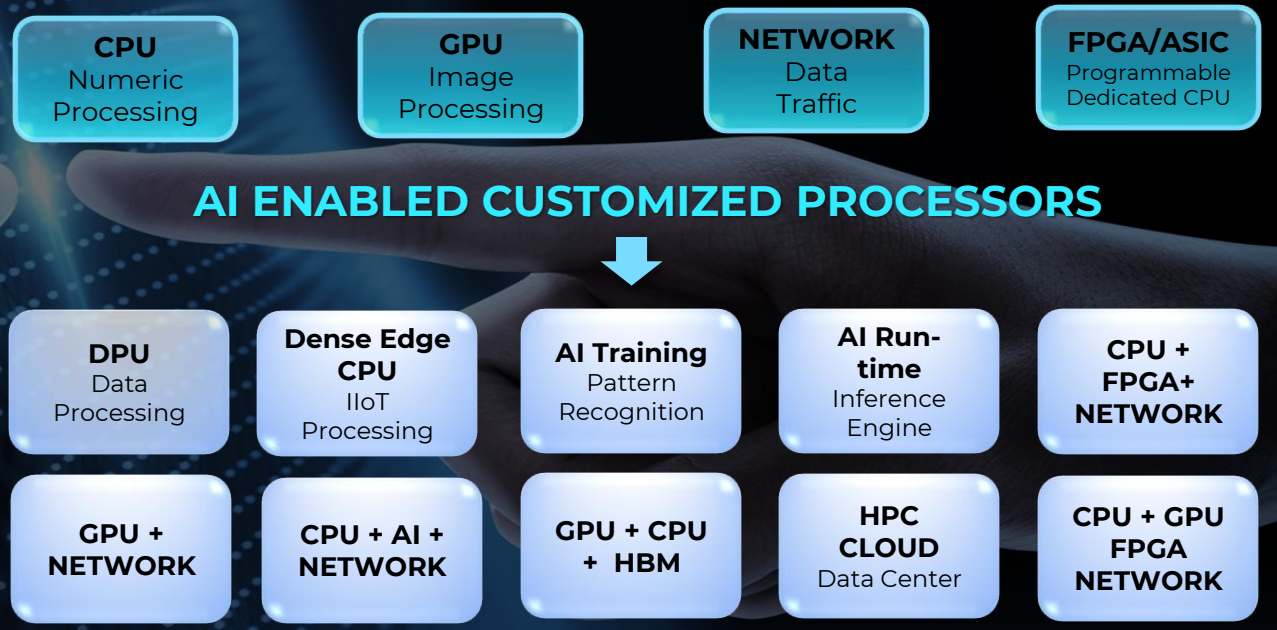
AI Will Drive, Like Never Before, Computing & Memory Needs, Customization

Integration of AI is Creating New Processor Structures

- Processor customization
- More powerful, efficient chips w/ higher bandwidth
- High degree of parallelism with multiple complex processing elements
- Higher adoption of AI Accelerators

Will Drive the Growth of Chiplets & Heterogeneous Integration

- Increased integration and multi-die packaging, heterogeneous integration
- Larger packages and more advanced substrates

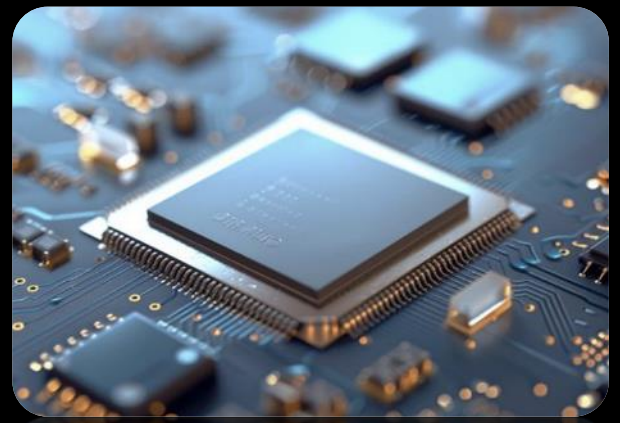


AI models in data centers are becoming more complex, driving the evolution of chip architecture

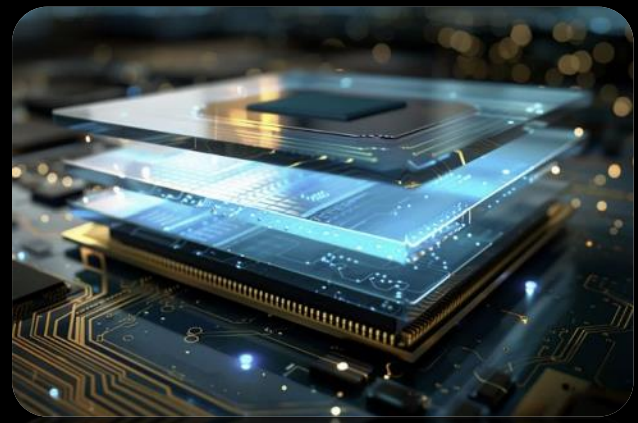
The Rise Of Chiplet Is Driving Advancements In Advanced Packaging

AI / HPC is Driving a Transformative Era in Chiplet Technology & Packaging

- **Chiplets:** a modular approach to system design that is performance driven and cost-effective, customizable and scalable to different computing applications
- The true potential of chiplets is unlocked through advanced packaging solutions and heterogeneous integration
- The economics of chiplet adoption are linked with the cost and maturity of the interconnect & packaging solutions



Single Chip FCBGA



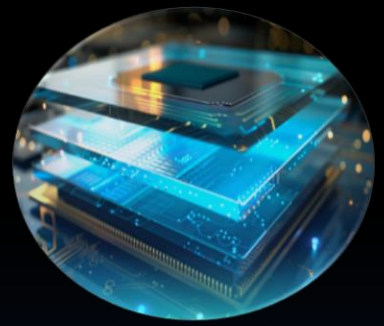
Multi-Chip / Chiplet Packaging

Chiplets Reshaping the Landscape of Advanced Packaging, Driving the Growth of Heterogeneous Integration

High Performance Processors Need High Performance IC Substrates

AI / HPC Driving the Trend Towards Significantly Bigger and More Complex Substrates

- Increased substrate size
- Increased layer count
- More advanced interconnects
- Embedding technologies
- Multi-core substrates
- Glass substrates



Chip I/O increasing is driving the need for finer pitches and denser interconnects in IC substrates, strongly pushing IC Substrate makers to reduce L/S interconnects and microvias

Computing Growing Exponentially, Faster than Interconnect Improvement & Developments

AI & HPC Driving The Need For More Advanced Interconnects

Substrate Interconnect Scale Roadmap

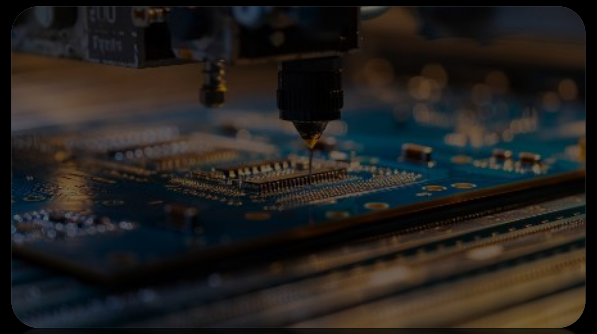
Source: IEEE, Georgia Tech, SEMI, 2022

Materials	Application	Min. Features (um)	2018	2020	2022	2025	2028	2031	2034
Organic Laminate	FCBGA	Bump Pitch	130/100 40/80 30/60	110/100 30/60 20/40	110/100 30/60 20/40	100/90 20/40 15/30	100/90 20/40 15/30	90/80 20/40 15/30	90/80 20/40 15/30
		L/S	9/12	9/12	8/8	5/5	5/5	5/5	5/5
		uVia Diam	50	50	40	30	30	20	20
	CHIPLET (fan-out, organic interposer)	Bump Pitch	50	50	45	40	40	30	30
		L/S	2/2	2/2	1.5/1.5	1/1	1/1	0.5/0.5	0.5/0.5
		uVia Diam	30	30	20	10	10	5	5
Silicon	CHIPLET (2.5D, 3D)	Bump Pitch	40	40	35	30	30	20	20
		L/S	0.6/0.6	0.6/0.6	0.6/0.6	0.5/0.5	0.4/0.4	0.3/0.3	0.2/0.2
		uVia diam	0.6	0.6	0.6	0.5	0.4	0.3	0.2

OUR STRATEGIC FOCUS: ULTRA HIGH END INTERCONNECTS

Presentation Agenda

Industry Trends



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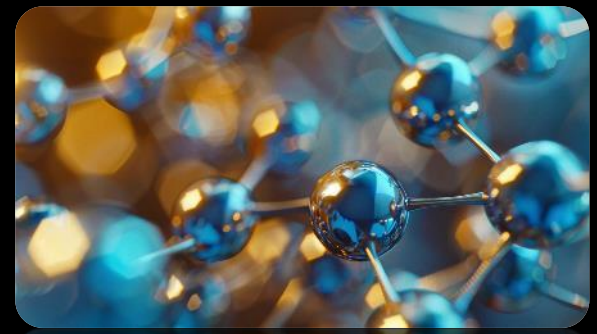


- High Density Interconnects
- The Road to 1um

A Silicon Valley Nanomaterials Company Focused On Interconnect Technologies for Advanced Packaging & Substrates

Incubated At Stanford Research Institute.

Engineered At Averatek / LQDX Santa Clara.

Patented Nano-Inks for AI & HPC Driven Advanced Semiconductor Interconnect

Our Patented Liquid Metal Ink (LMIx™) – Proven Technology That Meets Today The Needs Of Next Generation IC Substrates

- **Unique Atomic Seed Metallization** chemistry suite, enabling very uniform deposition of palladium, gold, copper and other semiconductor metals.
- **Palladium seed metal is the bedrock of every printed circuit made**, including the most advanced substrates, and **the roadmap demands feature sizes of <5um**.
- Our proven seed-metallization chemistries are a critical tool in the new Heterogeneous Integration toolbox. **LMI_X® has been proven on custom projects**: **our focus is now scaling it into the IC substrates, organic interposer and TSVs**

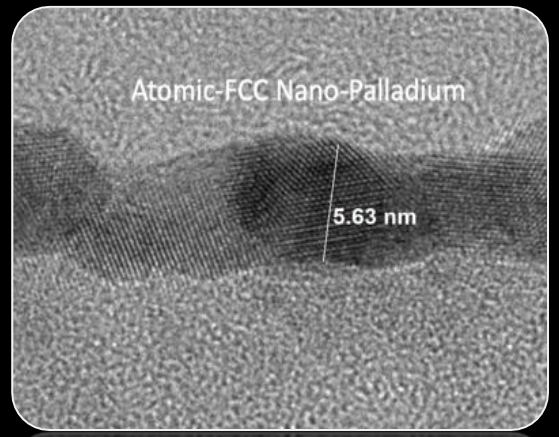
US PCB Capabilities
75/75um => 25/25um

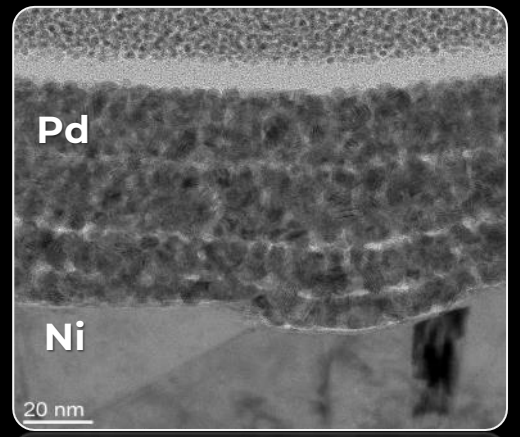
Advanced IC Substrates HVM (Asia)
8/8um

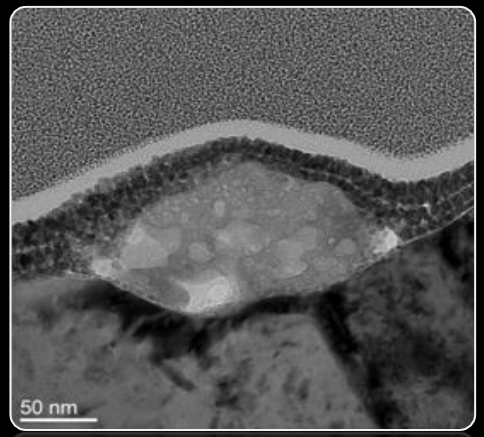
LQDX LMI
5/5um => 1um L/S

Nano Conformal Deposition Of Atomic Palladium

- Atomic Pd: very thin, nano-layers of conformal Pd deposition (≤ 5nm)
- Atoms will follow the contour very well
- Conformal – difficult to do with PVD

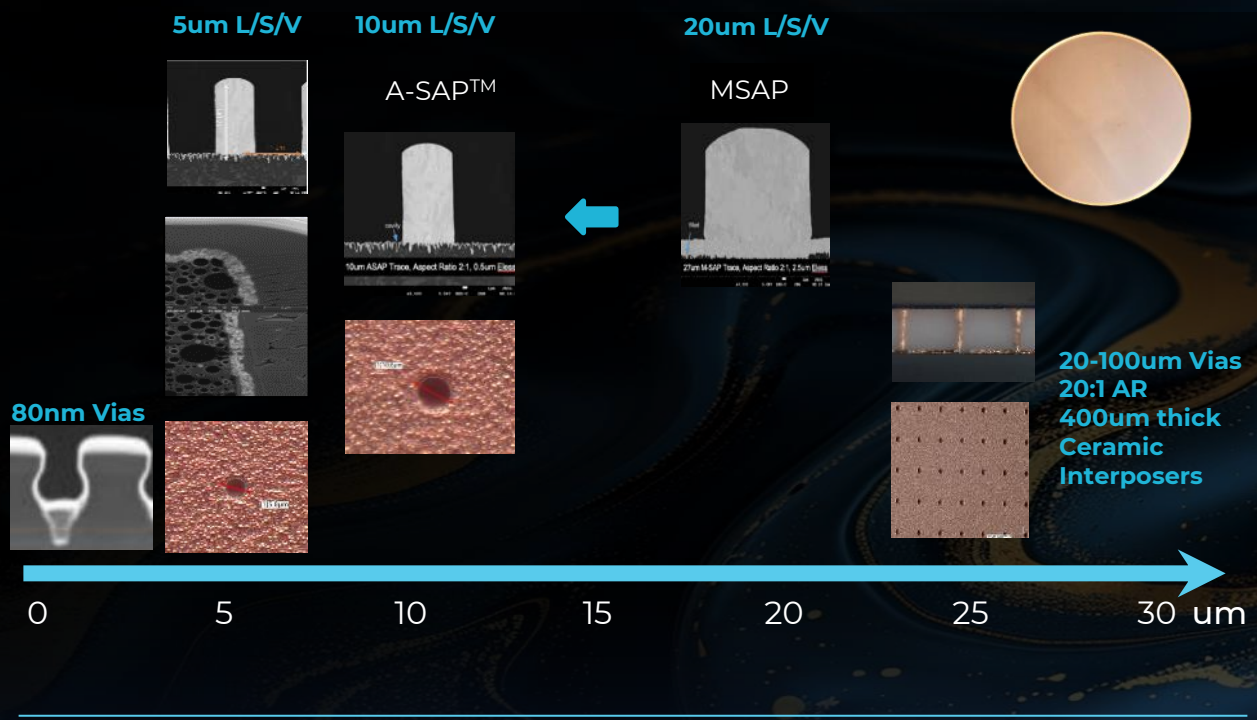






LMI Has a Molecular and Compositional Architecture that Enables Atomic Pd Deposition on the Nano Contours of Substrates

Enabling Advanced Circuits on the Largest Range of Substrates



- **Ultra Thin**: a few nanometers thick **(≤ 5nm Pd vs 100nm PVD)**
- **Ultra Dense**: fully packed nano film enabling uniform initiation of e-less copper **(80nm Cu vs 200-300nm PVD)**
- **Ultra Conformal**: complex surfaces at nanometer scale, **high AR (20:1)** features (TSVs)
- **Ultra Compatible**: adheres to advanced substrates and wide range of materials (Build-up Film, PID, LCP, BT, PTFE, Ceramics, FR4, Flex)
- **Ultra Flexible**: works with pure metals & alloys

Lowest Cost of Adoption And Easy Adoption & Integration into Existing Wet Processing Lines

Driven By Our Passion For Innovation & Engineering, We Are Pushing The Boundaries In Interconnect Technologies

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		uVia diam	0.6	0.6	0.6	0.5	0.4	0.3	0.2

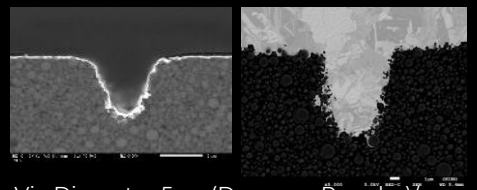
OUR STRATEGIC FOCUS: **Enabling The Roadmap to ≤1um L/S using Wet Processing**

The Roadmap To 1um

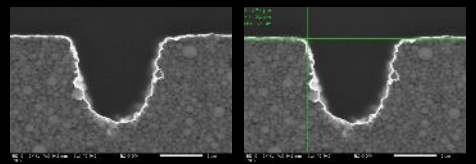
Building Integrated Process for Advanced Interconnects using Wet Process Seed Deposition

Test Vehicle Preparation → ABF Lamination → Via Formation → Desmear / Cleaning → Pd Catalyzation → E-less Cu → PR Patterning → Cu ECD → PR Removal → Seed Removal

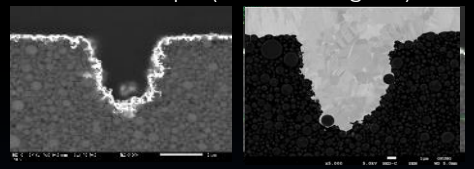
Via Diameter 5µm (Desmear Light)



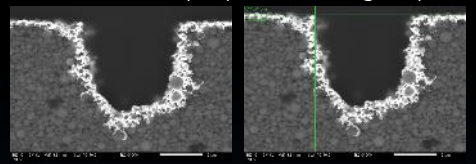
Via Diameter 8µm(Desmear Light)



Via Diameter 5µm(Desmear Regular)/



Via Diameter 8µm(Desmear Regular)



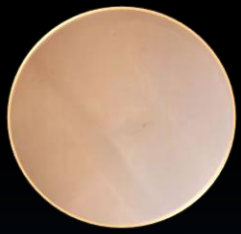
ABF Build up Film — AJINOMOTO

Pd Catalyzation — LQDX

E-less Cu — OKUNO (OKUNO CHEMICAL INDUSTRIES CO. LTD)

Integration of Process Steps & Materials & Characterization

- 1-5um L/S
- 5-20um microvias
- Via formation: using various technologies
- Patterning: stepper vs laser direct imaging
- Photoresist: dry and liquid films
- Electrical characterization & reliability testing



AJINOMOTO

LQDX

UYEMURA

ABF laminated wafers & seeded with 2nm Pd & 100nm E-less Cu
45nm roughness

Proven Solution in HVM and With Strong Partnership Engagements

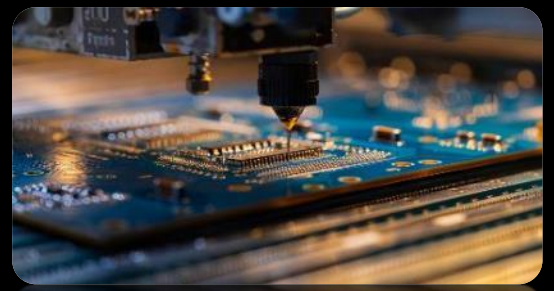
Meet Some of our Partners

U.S. AIR FORCE · UNITED STATES NAVY · ALCONIX · BOEING · BOSCH · brewer science · AJINOMOTO · OKUNO CHEMICAL INDUSTRIES CO. LTD. · FTG · LOCKHEED MARTIN · TAIYO · TE connectivity · Toyal · AZC · UYEMURA

We are fully equipped to get your design prototyped and into production for testing

Summary

Industry Trends



Current Challenges

LQDX Introduction

Our Solutions

- Exciting times in the semiconductor industry with multiple growth technologies ramping up
- AI & HPC are driving an unprecedented market inflection, and driving innovation at a rate of change the world has never seen before
- New materials and process tools are urgently needed in the industry toolbox to address the needs of AI and enable its growth
- While packaging technologies are available to address the needs of chiplets integration, they have high cost and are complex (2.5D)
- Increased adoption of chiplets & heterogeneous integration driving the need for larger, more complex and advanced substrates, finer interconnect solutions
- PDV adoption is being considered => higher cost, footprint and has its own challenges: less conformal, cannot address high-aspect-ratio features, thicker films
- LQDX has developed a suite of cutting edge technologies and processes and can bring a disruptive leap in interconnect technology.

Discover the Liquid-X Process that is Right For You

The Future of AI and HPC Substrates: A Breakthrough Interconnect Technology

For additional information:
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