

Organizing Committee

Habib Hichri



hichrih@aiiusa.com Executive VP Ajinomoto Fine Techno USA Corp



Rosalia Beica rozalia@LQDX.com **Chief Commercial Officer** LQDX



Annette Teng ateng@sunypoly.edu Director of Package Integration AIM Photonics, TAP Facilities

In person event

May 2nd-3rd 2024 SEMI, 673 S. Milpitas Blvd Milpitas, CA 95035

Jan Vardaman

President

Kuldip Johal

jan@techsearchinc.com

TechSearch International, Inc.

Kuldip.iohal@atotech.com

Global OEM Director

Farhang Yazdani

President & CTO

Paul Wesling P.wesling@ieee.org **Principal Engineer**

Hewlett-Packard Co (Retired)

Broadpak

MKS Instruments, Inc.



Venky Sundaram venky@3dsystemscaling.com Founder 3DSystemScaling



MattKelly@ipc.org CTO & VP Technology Solutions

Register at: www.ieee-

IEEE

SOCIETY

Farhang.Yazdani@broadpak.com

Steven Verhaverbeke Steven Verhaverbeke@amat.com Applied Materials

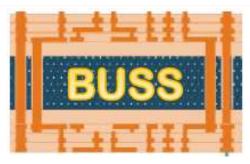
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8 8-4 - 1 8 8	May 2nd Thurs	Schedule	Speakers	Affiliation	Talk Title
	Opening	8:30am	Habib Hichri	Ajinomoto	Opening and BUSS program
BUSS	Keynote I	8:45am	Daniel Berger	NAPMP, Associate Director	Keynote:NAPMP Plans & Advanced Substrate Onshoring
	Keynote II	9:30am	D.C. Hu	SiPlus, Founder	2.XD Integrated Substrate Solutions for High Performance Computing
		10:15am T	Tea Break		
DAY 1 Program	Substrate Manufacturing &	11:00am	Sundar Kamath	Sanmina	An American PCB Manufacturer's Perspective on the Domestic Substrates Manufacturing Opportunity
May 2, 2024 at	Onshoring (Chair: Rozalia Beica)	11:20am	Meredith LaBeau	Calumet, CTO	Onshoring Organic Substrates (High-Density Build-Ups):A tale of Domestic Manufacturing & Title 3 Investments
SEMI		11:40am	Sung Jin Kim	Absolics, CTO	Packaging Substrate Solutions for Advanced Packaging Requirements
673 S. Milpitas Blvo	1	12:00pm	Michael Gleason	GreenSource Fabrication	DPA Title III Expansion Update
		12:20pm Lu	inch from Dish Dash		
Milpitas, CA 95035	Materials Advances for Substrates (Chair: Annette Teng)	1:30pm	Yishio Nishimura	Ajinomoto	Advanced Insulating Material for Next Generation Packaging
		1:50pm	Yuta Ogawa	Taiyo Ink	Taiyo's Photo-Dielectric for High Density Substrate Applications
		2:10pm	Fukui Masato	Resonac	Substrate Materials for Advanced Packaging
		2:30pm	Hikaru Mizuno	JSR Micro	Novel Low Loss Materials for Advanced IC Packaging
	Emerging Substrate	2:50pm	Steven Verhaverbeke	AMAT	Wafer Level Substrates – An Emerging New Technology
	Technologies	3:10pm	Farhang Yazdani	BroadPak	Advanced X64 UCIe Interface Implementatio on a Substrate
www.ieee-	(Chair: Steven Verhaverbeke)	3:30pm	Ken Yang,		Chiplet Integration on Organic Buildup with Silicon
buss.org			Vineeth Harish	UCLA	Interconnect Fabric
	"Substrate Needs:	3:50pm Tea	Sai Boyapati	AMD Sr Dir Adv Dkg	Substrate Needs: The User Perspective
	User Perspective"	4.50pm	Diane Peng	AMD, Sr. Dir. Adv. Pkg. Marvell	Substrate Needs. The Oser Perspective
ELECTRONICS	Panel session		Omar Bchir	Qualcomm	
PACKAGING	moderated by Jan		Susan Bagen	Raytheon, Microelectronics Cslt.	
SOCIETY	Vardaman		Jon Woodyard	Microsoft, Principal Engineer	
		5:30pm	,	itered by Armadillo Willy's	
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	May 3rd Friday	Schedule	Speakers	Affiliation	Talk Title
	Keynote I	9:00am	Venky Sundaram	3D System Scaling	USA Landscape for Substrate Manufacturing
	Keynote II	9:35am	Rahul Iyer	KCK Group	Venture Funding for startups
		10:10am	30 minutes Coffee/Tea break		
	Panel Equipment for Substrates (Chair: Kuldip	10:40am	Kyle Baker	MKS Instruments	QCW CO2 laser drilling for FCBGA applications.
	Johal)	11:00am	Takuma Yoshikawa	Nikko Materials	The Latest Vacuum Lamination Challenges and Technology
DAV 2 Program		11:20am	Frank Bruening	MSD-Atotech	Systems solutions for Advanced IC substrate manufacturing
DAY 2 Program May 3, 2024		11:40pm	Rozalia Beica	LQDX	The Future of AI and HPC Substrates: A Breakthrough Interconnect Technology
at		12:00pm	60 minutes Lunch		
	Panel Equipment and Technologies for	1:00pm	Harish V Penmethsa	Applied Materials	Metallization Technologies for Advanced Substrates
SEMI 673 S. Milpitas Blvd Milpitas, CA 95035	Substrates (Chair: Kuldip Johal)	1:20pm	Keith Best	Onto Innovation	Challenges for Organic & Glass Core Substrates as Advanced Packaging RDL Approaches < 2 μm L/S
	,	1:40pm	Gustavo Ramos	Green Source Engineering	Manufacturing with Zero Liquid Discharge (ZLD)
(m) = 2 (m)		2:00pm	Saminda Dharmarathna	MacDermid Alpha	Advanced Electroplating Processes for IC Substrates – Redistribution Layer and Embedded Trenches
		2:20pm	Purnima Narayanan	YES	Advanced packaging metallization-Substrate interaction with catalyst & electroless deposition of Cu
12884926		2:40pm	20 minutes Tea break		
- 5 5 b	Inspection and Testing	3:00pm	Robert Bishop	Beltonics	Advanced Metrology for High Density Substrates
	(Chair: Farhang Yazdani)	3:20pm	Orit Hava Armon Hershkovich	KLA Corporation	Inspection challenges in ICS & Advanced panel packaging markets
	"Empowering Startups in		Simon McElrea	LQDX	Empowering Startups in Advanced Substrates: A Key
www.ieee-buss.org	Advanced Substrates: A		Sam Salama	Hyperion	Component in US Onshoring
	Key Component in US Onshoring"	3:40pm-	Tristan O. El Bouayadi	Thintronics	Supply chain innovations
	Panel session moderated	4:40pm	Siddharth Ravichandran	Chipletz	Empowering Startups in Advanced Substrates: A Key
	by Venky Sundaram and		Brett Sawyer	Nubis Communications	Component in US Onshoring
PACKAGING	Kuldip Johal		Michael Gleason	GreenSource Fabrication	Substrate and Design Innovations
SOCIETY	Book Raffle & Closing	4:40pm	Habib Hichri	Ajinomoto Fine Techno USA Corp	Closing Remarks





DAY 1 TECHNICAL SESSION Substrate Manufacturing & Onshoring



Rozalia Beica rozalia@LQDX.com Chief Commercial Officer LQDX



IC Substrates, essential for the production of semiconductors and electronic devices, have historically been sourced from overseas markets, primarily in Asia. However, vulnerabilities exposed by supply chain disruptions have prompted a renaissance in domestic manufacturing initiatives. In this session, experts and industry leaders will address the role of technology and innovation in driving the substrate manufacturing and onshoring in US.

		Sched ule	Speakers	Affiliation	Talk Title
	manuracturin	11 Ulam	Sundar Kamath		An American PCB Manufacturer's Perspective on the Domestic Substrates Manufacturing Opportunity
	g & Onshoring (Chair: Rozalia	11:20am	Meredith LaBeau		Onshoring Organic Substrates (High-Density Build-Ups): A tale of Domestic Manufacturing & Title 3 Investments
	Beica)	11:40am	Sung Jin Kim		Packaging Substrate Solutions for Advanced Packaging Requirements
5		12.00pm	Michael	GreenSource Fabrication, Director Product Development	DPA Title III Expansion Update



DAY 1 TECHNICAL SESSION Materials Advances for Substrates

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May 2nd	Schedule	Speakers	Affiliation	Talk Title
Chair:	1:30pm			Advanced Insulating Material for Next Generation
Annette	1.00pm	Yishio Nishimura	Ajinomoto	Packaging
Teng	1:50pm			Taiyo's Photo-Dielectric for High Density
	1.50pm	Yuta Ogawa	TaiyoInk	Substrate Applications
	2:10pm	Fukui Masato	Resonac	Substrate Materials for Advanced Packaging
	2.20pm			Novel Low Loss Materials for Advanced IC
	2:30pm	Hikaru Mizuno	JSR Micro	Packaging

Annette Teng ateng@sunypoly.edu Director of Package Integration AIM Photonics, TAP Facilities

This session will focus on development of new organic dielectric materials for high density build-up substrate. There are challenges to find materials for thinner and stronger substrate while increasing the formfactor to support more and larger chiptets with good manufacturing yields and device performance. The race to find viable materials and processes with properties to support high transmission speed with low loss approaching <3um line space width will be presented.





DAY 1 TECHNICAL SESSION Emerging Substrate Technologies

May 2nd	Time	Speakers	Affiliation	Talk Title
Chair: Steven	2:50pm	Steven Verhaverbeke	AMAT	Wafer Level Substrates – An Emerging New Technology
Verhaverbek e	3:10pm	Farhang Yazdani		Advanced X64 UCIe Interface Implementatio on a Substrate
	3:30pm	Ken Yang, Vineeth Harish	UCLA	Chiplet Integration on Organic Buildup with Silicon Interconnect Fabric

This session will focus on Novel Substrate Technologies that have the potential to bring back Substrate Technologies to the USA. The first talk in this session will introduce Wafer-Level Substrates and contrast this against the current incumbent Panel-Level Substrates with existing installed base in Asia. The second talk in this session will introduce novel substrate finishing structures to enable die bumping on substrates with a <10um pitch. The final talk in this session will introduce novel technologies to enable UCIe connectivity between dies directly on substrates without any Si interposer or RDL interposer.



Steven Verhaverbeke <u>Steven Verhaverbeke@amat.com</u> Applied Materials





DAY 1 PANEL SESSION **Substrate Needs: The User**

	Moderator	Time	Panelist	Affiliation	Title
Mara N	Jan		Sai Boyapati	AMD	Senior Director Advanced Packaging
			D' D	Marvell	Senior Principal Engineer
			Omar Bchir		Senior Director of Engineering, Package Process &
					Technology
Jan Vardaman			Susan Bagen	Raytheon	Microelectronics Consultant
jan@techsearchinc.com President			Jon Woodyard	Microsoft	Principal Engineer

President TechSearch International, Inc.

Substrates are required to support high-performance compute and telecom, automotive electronic, consumer, defense, and medical applications. Regardless of the interposer technology, silicon or redistribution layer substrates, attachment to a build-up substrate creates the final package. There is also interest in continuing direct chip attach to a high-density organic substrate, with options including a glass core. This panel provides substrate user perspectives on feature size requirements today and tomorrow. Highlighted is a discussion on requirements to be a substrate supplier in the different applications. Reliability requirements and any special substrate needs are described. Consideration of geographic location for substrate suppliers is addressed.







Jan Vardaman jan@techsearchinc.com President TechSearch International, Inc.

Day 1 Panel session Substrate Needs: The User Perspective

Panelists from AMD, Marvell, Qualcomm, Raytheon & Microsoft will address topics on

- a) What substrate density is required to meet needs over the next few years for your applications? (L/S, Via/pad)
 - Does the use of an interposer reduce the demands on feature size?
- b) Where does glass core or glass substrate fit in advanced packaging and what are the key applications that will drive its development?
 - When do you expect this technology to be ready?
- c) What board-level reliability requirements to you require or do you look at BLR data when considering substrate supply? What other considerations are important to be a substrate supplier? Is geographic location a consideration?
- d) What process and metrology tools are needed to improve yield for large, high-layer count, high-density substrates?
- e) What is required to build a North American advanced packaging ecosystem that includes substrate manufacturing
 - What are the major challenges?



DAY 2 SESSION



Panel Equipment and Technologies for Substrates (Chair: Kuldip Johal) The focus of the session is equipment / processes used for IC substrate manufacturing for current POR HVM and next generation. We have leading industry experts from the supply chain to provide incite to IC substate tools.

May 3rd Friday	Schedule	Speakers	Affiliation	Talk Title
Panel Equipment	10:40am	Kyle Baker	MKS Instruments	QCW CO2 laser drilling for FCBGA applications.
and Technologies for Substrates	11:00am	Takuma Yoshikawa		The Latest Vacuum Lamination Challenges and Technology
(Chair Kuldip Johal)	11:20am	Frank Bruening		Systems solutions for Advanced IC substrate manufacturing
	11:40am	Rozalia Beica		The Future of AI and HPC Substrates: A Breakthrough Interconnect Technology
	12:00pm	60 minutes lunch		
Panel Equipment	1:00pm	Harish V Penmethsa	Applied Materials	Metallization Technologies for Advanced Substrates
and Technologies for Substrates	1:20pm	Keith Best		Challenges for Organic & Glass Core Substrates as Advanced Packaging RDL Approaches < 2 µm L/S
(Chair: Kuldip	1:40pm	Gustavo Ramos	Green Source Engineering	Manufacturing with Zero Liquid Discharge (ZLD)
Johal)	2:00pm	Saminda Dharmarathna		Advanced Electroplating Processes for IC Substrates – Redistribution Layer and Embedded Trenches
	2:20pm	Purnima Narayanan		Advanced packaging metallization-Substrate interaction with catalyst & electroless deposition of Cu



DAY 2 TECHNICAL SESSION INSPECTION AND TESTING

	May 3rd Friday	Schedule	Speakers	Affiliation	Talk Title
3	Inspection and Testing (Chair: Farhang)	3:00pm	Robert Bishop		Advanced Metrology for High Density Substrates
			o * 11		
			Orit Hava Armon Hershkovich		Inspection challenges in ICS & Advanced panel packaging markets
V					

Farhang Yazdani Farhang.Yazdani@broadpak.com President & CTO Broadpak



Venky Sundaram venky@3dsystemsc Founder 3D System Scaling



	DAY 2 PANEL SESSION
Emp	owering Startups in Advanced Substrates:
scaling.com	A Key Component in US Onshoring

A ff:l:ation

ob oystelli odalling	woderators	lime	Panelists	Affiliation	
			Simon McElrea	LQDX	Supply Chain
	Sundaram & Kuldip Johal	4:00pm- 5:00pm	Sam Salama	Hyperion	Innovations
			Tristan O. El Bouayadi	Thintronics	IIIIOvalions
			Siddharth Ravichandran	Chipletz	Substrate and
Kuldip.johal@atotech.com			Brett Sawyer	Nuble Communicatione	Design Innovations
Global OEM Director MKS Instruments, Inc.			Michael Gleason	Greensource	

In this panel session, we will convene a diverse group of US-based startups from across the package substrate value chain. The goal is to engage in an insightful discussion about the critical role these startups play in revitalizing US leadership in advanced packaging. The panel will feature perspectives from various angles:

Davallate

Madaratara Tim

Materials and Process Tool Startups: These startups provide essential tools and materials that enable the next generation of substrates. From novel manufacturing processes to advanced materials, they are attempting to disrupt the substrate supply chain.

New Substrate Design and Product Startups: These innovative companies are at the forefront of developing cutting-edge substrate designs and integrating advanced technologies such as photonics, contributing to innovations that drive power efficiency, performance enhancements, and miniaturization.

This interactive session with audience engagement will explore how startups are reshaping the landscape of advanced substrates and on shoring.

Raffle Drawing at 5:00pm May 3rd Must be present to win 2023 book Autographed by John Lau

Chiplet Design and Heterogeneous Integration Packaging

John H. Lau

🖉 Springer

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Raffle Drawing at 5:00pm May 3rd Must be present to win upcoming book By Dongkai Shangguan

To be Mailed direct to winner



Direct Copper Interconnection for Advanced Semiconductor Technology

Dongkai Shangguan

CRC Press

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Chapter 1	Advanced Packaging Landscape for Heterogeneous Integration
	Ravi Mahajan, Sairam Agraharam, Debendra Mallik, and Vijaya Boddu
Chapter 2	Direct Copper Interconnection for Die/Wafer Bonding: Overview
	Tzu-Heng Hung, and Kuan-Neng Chen
Chapter 3	Hybrid Bonding Process Technology
	Guilian Gao and Laura Mirkarimi
Chapter 4	Materials for Hybrid Bonding
	Andrea Chacko, Dongshun Bai, and Rama Puligadda
Chapter 5	Copper Electrodeposition for Advanced Packaging & Hybrid Bonding
	Bryan Buckalew
Chapter 6	Planarization for Advanced Packaging & Hybrid Bonding
	Brian J. Brown, Ekaterina Mikhaylichenko, Jianshe Tang, Jun Qian,
	and Yen-Chu Yang
Chapter 7	Permanent and Temporary Wafer Bonding
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Chapter 8	Die to Wafer Hybrid Bonding for Direct Copper Interconnection
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Chapter 9	Design for Hybrid Bonding and Chiplets
	Brandon Wang and Rong Bao
Chapter 10	Thermal Modeling and Simulation for Advanced 3DIC Systems
	Norman Chang, David Geb, Akhilesh Kumar, C.T. Wu, and Bo Ren
Chapter 11	Characterization, Modelling and Reliability for Direct Copper
	Interconnection
	Stephane Moreau and Dongkai Shangguan
Chapter 12	Applications of Hybrid Bonding and Chiplets for Heterogeneous Integratio
	Raja Swaminathan, John Wuu, Chandrasekhar Mandalapu, and Liwei Wang



